Intel® 440MX Scalable Low Power Development Kit

User's Manual

December 2001

Order Number: 273632-001

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Revision History

Revision	Date	Description
001	December 2001	First release of document.

About This Manual 1

This manual tells you how to set up and use the evaluation board and processor assembly included in your Intel® 440MX Scalable Low Power Development Kit.

1.1 Content Overview

Chapter 1, “About This Manual” — This chapter contains a description of conventions used in this manual. The last few sections tell you how to obtain literature and contact customer support.

Chapter 2, “Getting Started”— Provides complete instructions on how to configure the evaluation board and processor assembly by setting jumpers, connecting peripherals, providing power, and configuring the BIOS.

Chapter 3, “Theory of Operation” — This chapter provides information on the system design.

Chapter 4, “Hardware Reference” — This chapter provides a description of jumper settings and functions, and pinout information for each connector.

Chapter 5, “BIOS Quick Reference” — This chapter describes how to configure the BIOS for your system configuration. A summary of all BIOS menu options is provided.

Appendix A, “Bill of Materials” — This appendix contains the bill of materials for the evaluation board.

Appendix B, “Schematics” — This appendix contains schematics for selected connectors and subsystems for the evaluation board.

1.2 Text Conventions

The following notations may be used throughout this manual.

#	The pound symbol (#) appended to a signal name indicates that the signal is active low.
Variables	Variables are shown in italics. Variables must be replaced with correct values.
Instructions	Instruction mnemonics are shown in uppercase. When you are programming, instructions are not case-sensitive. You may use either upper- or lowercase.

Numbers

Hexadecimal numbers are represented by a string of hexadecimal digits followed by the character *H*. A zero prefix is added to numbers that begin with *A* through *F*. (For example, *FF* is shown as *0FFH*.) Decimal and binary numbers are represented by their customary notations. (That is, 255 is a decimal number and 1111 1111 is a binary number. In some cases, the letter *B* is added for clarity.)

Units of Measure

The following abbreviations are used to represent units of measure:

A	amps, amperes
Gbyte	gigabytes
Kbyte	kilobytes
KΩ	kilo-ohms
mA	milliamps, milliamperes
Mbyte	megabytes
MHz	megahertz
ms	milliseconds
mW	milliwatts
ns	nanoseconds
pF	picofarads
W	watts
V	volts
µA	microamps, microamperes
µF	microfarads
µs	microseconds
µW	microwatts

Signal Names

Signal names are shown in uppercase. When several signals share a common name, an individual signal is represented by the signal name followed by a number, while the group is represented by the signal name followed by a variable (*n*). For example, the lower chip-select signals are named CS0#, CS1#, CS2#, and so on; they are collectively called CS*n*#. A pound symbol (#) appended to a signal name identifies an active-low signal. Port pins are represented by the port abbreviation, a period, and the pin number (e.g., P1.0).

1.3 Technical Support

1.3.1 Electronic Support Systems

Intel's site on the World Wide Web (http://www.intel.com/) provides up-to-date technical information and product support. This information is available 24 hours per day, 7 days per week, providing technical information whenever you need it.

1.3.2 Telephone Technical Support

In the U.S. and Canada, technical support representatives are available to answer your questions between 5 a.m. and 5 p.m. PST. You can also fax your questions to us. (Please include your voice telephone number and indicate whether you prefer a response by phone or by fax). Outside the U.S. and Canada, please contact your local distributor.

1-800-628-8686	U.S. and Canada
916-356-7599	U.S. and Canada
916-356-6100 (fax)	U.S. and Canada

1.4 Product Literature

You can order product literature from the following Intel literature centers.

1-800-548-4725	U.S. and Canada
708-296-9333	U.S. (from overseas)
44(0)1793-431155	Europe (U.K.)
44(0)1793-421333	Germany
44(0)1793-421777	France
81(0)120-47-88-32	Japan (fax only)

1.5 Related Documents

Table 1. Related Documents

Document Title	Order Number
Intel Pentium® III Processor Low Power datasheet	273500
Intel® Pentium® III Processor Specification Update	244453
Intel® Pentium® III Processor Thermal Design Guide	273325
Intel® Celeron® Processor Low Power/Ultra Low Power datasheet	273509
Intel® Celeron® Processor Specification Update	243748
P6 Family of Processors Hardware Developer's Manual	244001
Intel Architecture Software Developer's Manual, Volume1: Basic Architecture	243190
Intel Architecture Software Developer's Manual, Volume 2: Instruction Set Reference Manual	243191
Intel Architecture Software Developer's Manual, Volume 3: System Programming Guide	243192
Intel Processor Serial Number application note	245125

Getting Started 2

This chapter identifies the evaluation kit's key components, features and specifications. It also tells you how to set up the board for operation.

2.1 Overview

The evaluation board consists of a baseboard (with one Intel® Pentium® III processor populated), 440MX chipset, and other system board components and peripheral connectors.

Note: The evaluation board is shipped as an open system allowing for maximum flexibility in changing hardware configuration and peripherals. Since the board is not in a protective chassis, take extra precaution when handling and operating the system.

2.1.1 Baseboard Features

The evaluation board features are summarized below:

CPU

- Supports both Intel® Celeron® processors low power/ultra-low power (300 MHz and above) and Intel® Pentium® III processors low power (up to 700 MHz); both in the micro-PGA package.
- Supports a 66 or 100 MHz processor system bus (PSB).

Intel 440MX Chipset

- 82443MX PCIset
- Integrated IDE controller for Ultra DMA/33 Synchronous DMA mode

Memory Support

- 100 MHz system memory interface
- Two 168-pin DIMM sockets support SDRAM (3.3 V, non-ECC) modules
- Supports 8-Mbyte to 256-Mbyte using 16 Mbit/64 Mbit/128 Mbit technology

Flash System BIOS ROM

- General Software system BIOS

Power Supply/Management

- Standard ATX power supply connector
- SMRAM space remapping to A0000H (128 Kbyte)
- Optional Extended SMRAM space above 256 Mbyte, additional 512 Kbyte/1 Mbyte TSEG from top of memory, cacheable
- Stop clock grant and halt special cycle translation from the host to the hub interface
- APIC buffer management

System I/O

- One floppy connector supporting up to 2.88 Mbytes, and three-mode floppy drives
- One Ultra ATA 100/66/33 IDE connector supporting up to two IDE devices
- Built-in standard/EPP/ECP parallel port connector
- Two built-in 16550 fast UART compatible serial port connectors
- Two built-in Universal Serial Bus (USB) connectors
- Built-in PS/2-style keyboard and PS/2 mouse (6-pin mini-DIN) connectors
- Built-in audio connectors (Line-in, Line-out, MIC-in) with Sigmatel CODEC

Peripheral Connectors

- Three PCI expansion slots

Miscellaneous Features

- Micro ATX form factor
- Two built-in SMBus headers
- Built-In standard IrDA TX/RX header
- One built-in FAN power connector
- Power/Reset jumpers
- Jumper to clear CMOS

2.2 Included Hardware

- Evaluation board (baseboard) with battery
- One 500, 700 MHz Intel® Pentium® III Processor Low Power with a 100 MHz PSB
- One 300 MHz Intel® Celeron® Processor Ultra Low Power with a 100 MHz PSB
- One fansink thermal solution
- One 128-Mbyte PC100 SDRAM (168-pin)

- ATA66 hard disk drive pre-loaded with an evaluation copy of Hard Hat* from MontaVista*
- 80-pin ATA/66 IDE cable for the hard disk drive
- Intel 69000 graphics card

2.3 Software Key Features

The software in the kit was chosen to facilitate development of real-time applications based on the components used in the evaluation board. The software tools included in your kit are described in this section.

Note: Software in the kit is provided free by the vendor and is only licensed for evaluation purposes. Refer to the documentation in your evaluation kit for further details on any terms and conditions that may be applicable to the granted licenses. Customers using the tools that work with Microsoft* products must license those products. Any targets created by those tools should also have appropriate licenses. Software included in the kit is subject to change.

Refer to http://developer.intel.com/design/intarch/devkits for details on additional software from other third-party vendors.

2.3.1 Embedded BIOS for the Intel® 440MX Scalable Low Power Development Kit

The Intel® 440MX Scalable Low Power Development Kit ships pre-installed with Embedded BIOS* pre-boot firmware from General Software. Embedded BIOS provides an industry-standard BIOS platform to run any standard operating system, including DOS*, Windows* NT, NT Embedded*, Windows 95/98, Windows CE, QNX*, VxWorks*, and Linux* among others. The Embedded BIOS Application Kit (available through General Software) includes complete source code, a reference manual, and a Windows-based expert system, BIOStart*, to enable easy and rapid configuration of customized firmware for your Intel**®** 440MX Scalable Low Power Development Kit.

The following features of Embedded BIOS have been enabled in the Intel® 440MX Low Power Development Kit:

- SDRAM detection, configuration, and initialization
- Intel® 440MX chipset configuration
- Post codes displayed to port 80H
- Two serial ports, one EPP/ECP parallel port
- PCI bus and device enumeration and configuration
- SMC LPC Super I/O programming
- Pentium® III processor microcode update
- Integrated debugger
- Burn-in diagnostics
- Console redirection
- Manufacturing mode

2.3.2 Software

2.3.2.1 Hard Hat* Linux

The drive comes pre-loaded with Hard Hat Linux. Some of the features of Hard Hat Linux include:

Hard Hat Linux is a cross development platform and a set of tool kits designed specifically for embedded solutions.

Hard Hat Linux is designed for the scalability, dependability and performance required of well-designed embedded applications. Hard Hat Linux includes more than 75 Linux Support Packages (LSPs), 200+ software packages plus a comprehensive set of development tools.

MontaVista Software also makes available valuable technology add-on packages that address specific customer requirements such as the Java development environment, High Availability technology, GUI toolkit and more.

Hard Hat Linux supports a variety of capabilities exclusively for embedded applications. Technologies such as special back-plane communication for CompactPCI allow multiple board-level systems to communicate over a common bus interface. Support for headless operation enables the embedding of Linux in a video display, keyboard or mouse. Networks can be installed and booted without the need for rotating media. The Flash memory file system supports rugged solid-state storage needed for very small consumer devices. Run-time instrumentation makes it easy to monitor system integrity and performance. Hard Hat Linux also includes scaling and configuration tools that let developers right-size Linux kernel and filesystems to suit their memory footprint.

2.3.2.2 Wind River's VxWorks* Real-Time Operating System (RTOS)

Wind Microkernel

- Efficient task management
  - — Multitasking, unlimited number of tasks
  - — Preemptive and round-robin scheduling
  - — Fast, deterministic context switching
  - — 256 priority levels
- Fast, flexible intertask communications
  - — Binary, counting and mutual exclusion semaphores with priority inheritance
  - — Message queues
  - — POSIX pipes, counting semaphores, message queues, signals and scheduling
  - — Control sockets
  - — Shared memory
- High scalability
- Incremental linking and loading of components
- Fast, efficient interrupt and exception handling

- Optimized floating-point support
- Dynamic memory management
- System clock and timing facilities

Networking Support

- BSD 4.4 TCP/IP networking
- IP, IGMP, CIDR, TCP, UDP, ARP
- RIP v.1/v.2
- Standard Berkeley sockets, zbufs (a.k.a., zero-copy sockets)
- SLIP, CSLIP, PPP
- BOOTP, DNS, DHCP, TFTP
- NFS, ONC RPC
- FTP, rlogin, rsh, telnet
- SNTP
- WindNet SNMP v.1/v.2c with MIB compiler—optional
- WindNet OSPF v.2—optional

Fast, Flexible I/O and Local File System

- SCSI support
- MS-DOS compatible file system
- Raw disk file system
- TrueFFS flash file system—optional
- ISO 9660 CD-ROM file system
- PCMCIA support

Target Development Features

- Full ANSI C compliance and enhanced C++ features for exception handling and template support
- Extensive POSIX 1003.1, .1b compatibility
- Interactive C interpreter target shell
- Symbolic debugging and disassembly
- Powerful performance monitoring
- Extensive kernel, task and system information utilities
- Dynamic linking loader
- Libraries of over 1800 utility routines
- Flexible booting from ROM, local disk, or over the network
- Highly scalable design allows for a wide range of applications
- System-level debugging via Ethernet, serial line, ICE, or ROM emulator

Supported VxWorks 5.x Targets

- PowerPC
- 68K, CPU 32
- ColdFire
- MCORE
- 80x86 and Pentium
- i960
- ARM and StrongARM
- MIPS
- SH
- SPARC
- NEX V8xx
- M32 R/D
- RAD6000
- ST 20
- TriCore

2.4 Before You Begin

Before you set up and configure your evaluation board, you may want to gather some additional hardware and software.

VGA Monitor: You can use any standard VGA or multi-resolution monitor. The setup instructions in this chapter assume that you are using a standard VGA monitor.

Keyboard: You need a keyboard with a PS/2-style connector or adapter.

Mouse: Optional. You can use a mouse with a PS/2-style connector or adapter.

Hard Drives andFloppy Drives: You can connect up to two IDE drives and one floppy drive to the evaluation board. Two devices (master and slave) can be attached to the IDE connector. Only one hard drive is included in your kit, so you will need to provide the cables for any additional drives. You may have all these storage devices attached to the board at the same time. The compact flash is considered an IDE device, so only the compact flash and one IDE hard drive can be used at the same time.

Video Adapter: You must install a PCI video adapter. It is your responsibility to install the correct driver software for any video adapters.

Network Adapter: The network adapter is already installed on the board. You may use a different network card other than the one included in the kit; you are responsible for installing the correct drivers for such a network card. The evaluation board supports all standard PCI-compatible network cards. You must supply a network cable to connect to the LAN connector or any other network card you chose to install.

Power Supply: You must use a standard ATX power supply.

Other Devices and Adapters: The evaluation board functions much like a standard desktop computer motherboard. Most PC compatible peripherals can be attached and configured to work with the evaluation board.

2.5 Setting up the Evaluation Board

Once you have gathered the hardware described in section Section 2.4, follow the steps below to set up your evaluation board. This manual assumes you are familiar with the basic concepts involved with installing and configuring hardware for a personal computer system. Refer to Figure 6 on page 32 for locations of connectors, jumpers, etc.

1. Create a safe work environment.

   Make sure you are in a static-free environment before removing any components from their anti-static packaging. The evaluation board is susceptible to electrostatic discharge damage, and such damage may cause product failure or unpredictable operation.

2. Inspect the contents of your kit.

   Check for damage that may have occurred during shipment. Contact your sales representative if any items are missing or damaged.

Caution: Connecting the wrong cable or reversing the cable can damage the evaluation board and may damage the device being connected. Since the board is not in a protective chassis, use caution when connecting cables to this product.

Note: The evaluation board is a standard micro-ATX form factor. An ATX chassis may be used if a protected environment is desired.

3. Check the jumper settings.

   CMOS jumper is used to clear the CMOS memory (pin 2 and 3). Make sure this jumper is set for normal operation (jumper pins 21 and 22). Refer to Section 4.3.1, “CMOS Jumper” on page 39.

4. Make sure the following hardware is populated on your evaluation board:

   — One Intel® Pentium® III processor

   — One 128-Mbyte PC100 SDRAM DIMM (168-pin)

   — One fan (thermal solution)

5. Install the IDE hard disk drive included in your kit:
   The evaluation board supports Primary and Secondary IDE interfaces that can each host one or two devices (master/slave). When you are using multiple devices, such as a hard disk and a CD-ROM drive, make sure the hard disk drive has a jumper in the master position and the CD-ROM has a jumper in the slave position. When using a single IDE device with the evaluation board, ensure that the jumpers are set correctly for single drive operation. For jumper settings for different configurations, consult the drive’s documentation.

   — Connect the hard drive’s IDE cable connector to the IDE1 connector on the evaluation board.

   — Connect the other end of the cable to the hard disk drive.

— Connect a power cable to the hard drive.

Caution: Make sure the tracer on the ribbon cable is aligned with pin 1 on both the hard disk and the IDE connector header. Connecting the cable backwards can damage the evaluation board or the hard disk.

6. Connect any additional storage devices to the evaluation board.

Note: The hard disk is already formatted and is pre-loaded with a customized target image of Hard Hat Linux by Montavista.

7. Connect a Floppy drive (optional).
   — Insert a floppy cable into FDC1 (be sure to orient pin 1 correctly).
   — Connect the other end of the ribbon cable to the floppy drive.
   — Connect a power cable to the floppy drive.
8. Connect the keyboard and mouse.
   Connect a PS/2-style mouse and keyboard (see Figure 6 on page 32 for connector locations).

Note: The bottom connector is for the keyboard and the top is for the mouse.

9. Connect the Ethernet adapter provided in your kit (optional).
10. Connect the audio speakers (optional).
    For audio, connect the audio speakers to the on-board line out connector.
11. Connect the power supply.
    Connect an ATX power supply to the evaluation board. Make sure the power supply is not plugged into the wall (turned off). Insert the board connector of the power supply cord into the ATXPR1 power supply header on the evaluation board. After connecting the power supply board connector to the ATXPR1 header, plug the power supply cord into the wall.
12. Power up the board.

Power and reset are implemented on the evaluation board through jumpers located on PN1 and PN2.

Power Jumper:	The power jumper consists of pins 5 and 7 on the front panel connector. To power on the evaluation board, briefly short pins 5 and 7, then, release the short. (To power off, short pins 5 and 7 for about five seconds, until the power shuts off.)
Reset Jumper:	The reset jumper consists of pins 1 and 3 on the front panel connector. To reset the evaluation board, short pins 1 and 3 until the board resets, and then release the short.

Turn on the power to the monitor and evaluation board. Ensure that the fansink on the processor is operating.

2.6 Configuring the BIOS

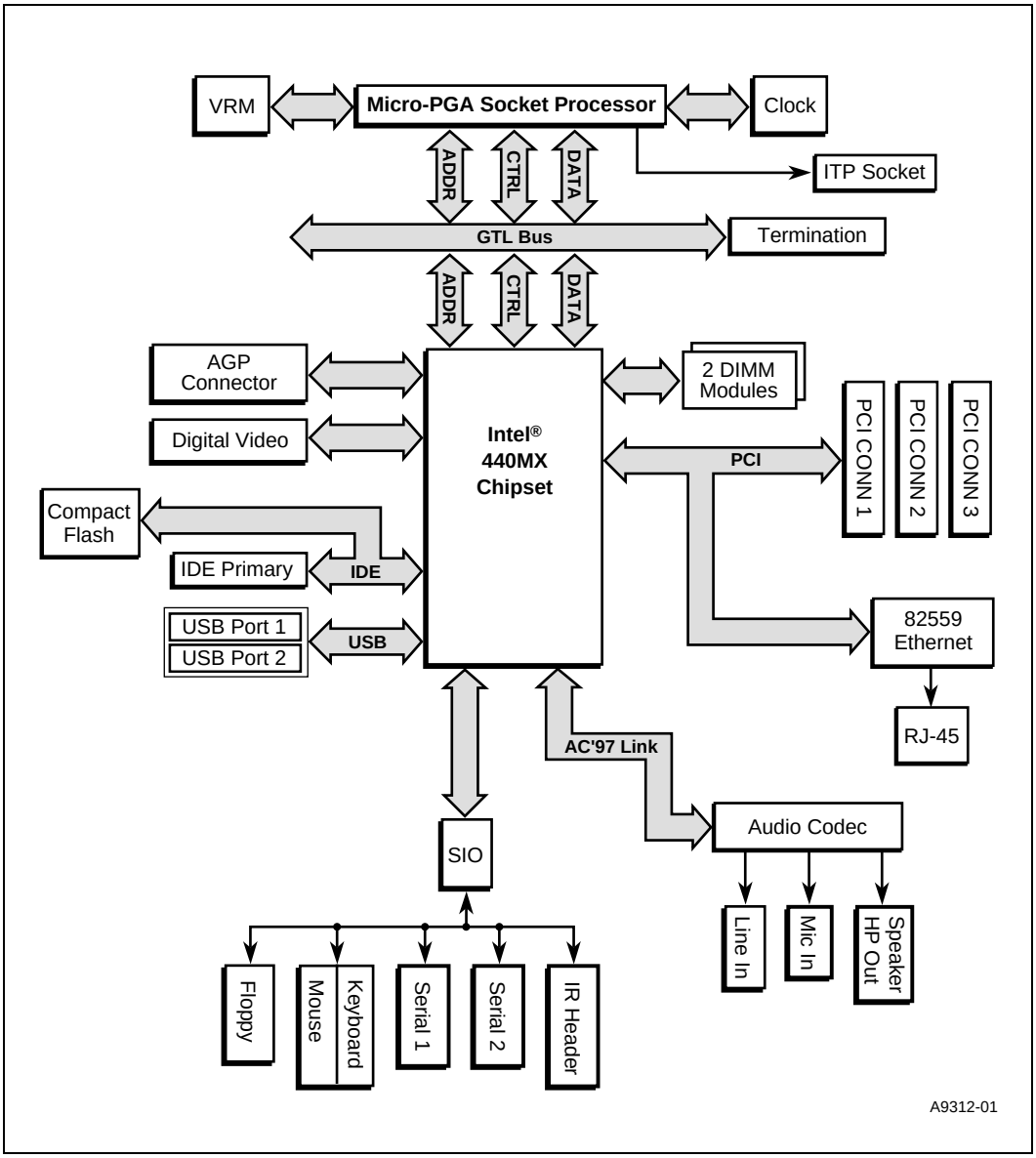
General Software's BIOS is pre-loaded on the evaluation board. You will need to make changes to the BIOS to enable hard disks, floppy disks and other supported features. You can use the Setup program to modify BIOS settings and control the special features of the system. Setup options are configured through a menu-driven user interface. Chapter 5, "BIOS Quick Reference" contains a description of BIOS options. BIOS updates may periodically be posted to Intel's Developers' Web site at:

http://developer.intel.com/design/intarch/devkits/

Theory of Operation 3

3.1 Block Diagram

Figure 1. Block Diagram



3.2 Mechanical Design

The evaluation board conforms to the micro-ATX form factor. For extra protection in a development environment, you may want to install the evaluation board in an ATX chassis. The evaluation board has three 32 bit/33 MHz PCI connectors, one AGP connector, one CNR connector, two SDRAM DIMM connectors, and one ABIT V-Bus connector. The system I/O connectors are in the rear of the board in the defined micro-ATX I/O window.

3.3 Thermal Management

The objective of thermal management is to ensure that the temperature of each component is maintained within specified functional limits. The functional temperature limit is the range within which the electrical circuits can be expected to meet their specified performance requirements.

Operation outside the functional limit can degrade system performance and cause reliability problems.

The development kit is shipped with a heatsink/fan thermal solution pre-installed on the processor using metal clips. This thermal solution has been tested in an open air environment at room temperature and is sufficient for evaluation purposes. The designer must ensure that adequate thermal management is provided for any customer-derived designs.

3.4 System Operation

The Intel® 440MX Scalable Low Power Development Kit is designed to support Intel® Celeron® processors low power/ultra low power (300 MHz and above) and Intel® Pentium® III processors low power up to 700 MHz in the BGA2 package. The 440MX chipset includes the GMCH, ICH2, and the FWH.

3.4.1 Intel® Pentium® III Processor

The Intel® Pentium® III processor is a member of the P6 family in the Intel® IA-32 processor line. Like the Intel® Pentium® II processor, the Intel® Pentium® III processor implements the Dynamic Execution microarchitecture — a unique combination of multiple branch prediction, data flow analysis, and speculative execution. Intel® Pentium® III processor features include the following:

- Dynamic Execution technology
- Includes Intel MMX media enhancement technology
- Intel streaming SIMD extensions
- Incorporates separate 16 Kbyte level-one caches (32 Kbytes total); one for instructions and one for data
- 256 Kbytes integrated, full-speed level two cache with error correcting code (ECC)
- 8-way level two cache associativity, which provides improved cache-hit rate on read/store operations
- Double quad word-wide (256 bit) cache data bus, which provides extremely high throughput on read/store operations

- Support for 66 MHz and 100 MHz processor system bus frequencies
- Intel® processor serial number

3.4.2 Intel® Celeron® Processor

The Intel® Celeron® processor family delivers quality, reliability, and compatibility while offering good performance for today's most widely-used applications. Intel® Celeron® processor features include:

- Dynamic Execution technology
- Includes Intel MMX* media enhancement technology
- Intel streaming SIMD extensions
- Incorporates separate 16 Kbyte level-one caches (32 Kbytes total); one for instructions and one for data
- Incorporates a 128 Kbyte unified, non-blocking, level-two cache that improves performance by reducing the average memory access time and providing fast access to recently used instructions and data
- 66/100 MHz Intel® P6 micro-architecture's multi-transaction system bus that supports multiple outstanding transactions to increase bandwidth availability
- A pipelined Floating-Point Unit (FPU) for supporting the 32-bit and 64-bit formats specified in IEEE standard 754, as well as an 80-bit format
- Parity-protected address/request and response system bus signals with a retry mechanism for high data integrity and reliability

3.4.3 Intel® 440MX Chipset

Features:

- 492 BGA package
- 66 or 100 MHz Processor System Bus
- 32-bit host bus addressing
- Four deep in-order queue
- Processor support
  - — Celeron® processor low power/ultra low power (128 Kbytes) in a micro-PGA package
  - — Pentium® III processor low power (256 Kbytes) in a micro-PGA package
- System DRAM controller
  - — Two DIMM slots
  - — 100 MHz clock

3.4.4 System Memory SDRAM

Memory Features:

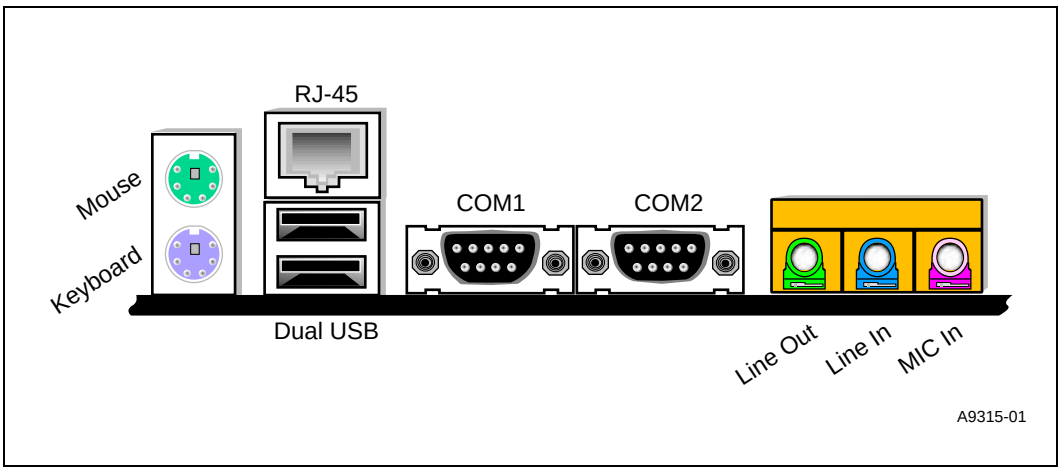
- Two 168-pin SDRAM DIMM sockets
- Supports 8 Mbyte to 256 Mbyte using 16 Mbit/64 Mbit/128 Mbit/256 Mbit technology
- Supports 100 MHz system memory bus

3.4.5 System I/O

The evaluation board contains the following I/O devices.

- Single floppy controller support
- Primary and secondary IDE interface (supports two drives)
- Two serial ports
- Two USB ports
- AC'97 specification compliant audio
- Speaker Out, Line IN, and MIC IN connectors
- PS/2-style keyboard and mouse ports
- IR header

Figure 2. Back Panel I/O Connectors



3.4.5.1 Floppy Disk Drive Support

One 34-pin floppy connector is provided on the evaluation board.

3.4.5.2 IDE Support

The evaluation board supports a primary IDE interface via a 40-pin IDE connectors.

3.4.5.3 RS-232 Serial Ports

The evaluation board provides two built-in serial ports (COM1 and COM2).

3.4.5.4 USB Ports

The evaluation board provides two USB connectors (USB1).

3.4.5.5 Audio Subsystem

The evaluation board has an integrated (on-board) AC'97 compliant subsystem.

Audio Subsystem Features:

- Line input (back panel)
- Speaker output (back panel)
- Microphone input (back panel)

3.4.5.6 Keyboard/Mouse

The keyboard and mouse connectors are PS/2 style, 6-pin stacked miniature DSUB connectors. The top connector is for the mouse and the bottom connector is for the keyboard.

3.4.5.7 IR Header

The evaluation board provides one IR header. The IR header can be used in place of COM2. To use the IR header, the BIOS vendor must modify the BIOS to activate IR and deactivate COM2. Contact either General Software or your own BIOS vendor to assist with the modification.

3.4.6 Expansion Connectors

The evaluation board contains the following expansion connectors:

- Three PCI 32/33 slots
- One compact flash slot
- Two SMBus headers

3.4.6.1 32-bit/33-MHz PCI Connectors

Three industry standard 32-bit/33-MHz PCI connectors (PCI1, PCI2, and PCI3) are provided on the evaluation board.

3.4.6.2 Compact Flash Slot

One compact flash slot is included on the board. The compact flash can be used as the IDE master with the proper jumper setting.

3.4.7 Post Code Debugger

An on-board Post-Code Debugger is implemented on the evaluation board.

3.4.8 Clock Generation

The clock synthesizer on the baseboard generates and distributes the clocks used by the entire system.

3.4.8.1 System Clocks

The CK Intel® 815E Chipset: 3 DIMM Clock Synthesizer is the primary source of clock generation for most of the clocks on the baseboard. The following clock groups are found on the Intel® 815E Scalable Performance Board Development Kit:

CPU	66 MHz/100 MHz
PCI	33 MHz
SDRAM	100 MHz
3V66	66 MHz (3.3 V)
USB	48 MHz
DOT	48 MHz
REF	14.31818 MHz
APIC	33 MHz

3.4.9 Power Supply Requirements

The Intel® 440MX Scalable Low Power Development Kit uses a standard ATX power supply.

3.5 Battery Requirements

A type 2032, socketed, 3 V lithium coin cell battery is used on this evaluation board. The battery has a shelf life of greater than three years.

Hardware Reference 4

This section provides reference information on the hardware, including connector pinout information and jumper settings.

4.1 Thermal Management

The development kit is shipped with a heatsink/fan thermal solution pre-installed on the processor using metal clips. This thermal solution has been tested in an open-air environment at room temperature and is sufficient for evaluation purposes. The designer must ensure that adequate thermal management is provided for any customer-derived designs.

For additional thermal design information refer to the following documents:

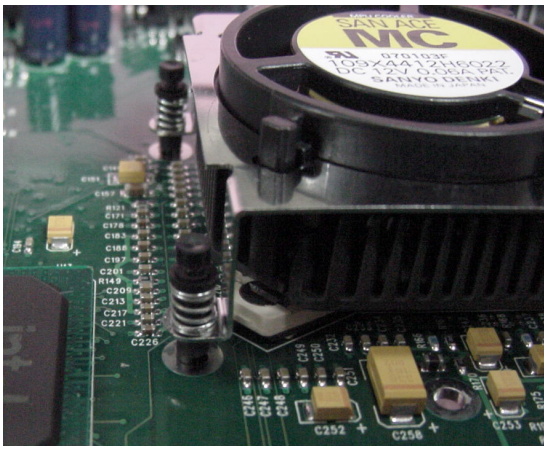
- *Pentium® III Processor for the PGA370 Socket at 500 MHz to 1.0B GHz Datasheet* (order number 245264)
- *Intel® Pentium® III Processor Thermal Design Guide* (order number 273325)
- *Intel® Celeron® Processor up to 850 MHz* datasheet (order number 243658)
- *Intel® Celeron® Processor Thermal Design Guide (*order number 273421)

4.1.1 Changing the Processor

If you wish to change the processor, follow these instructions to remove the heat sink assembly.

1. Disconnect the fan cable from the ATX power supply.
2. Remove the pins from the body on the four attachment rivets (see Figure 3) with needle-nose pliers.

Figure 3. View of the Fan/Heat Sink



3. Remove the body of the attachment rivets with needle-nose pliers.

Warning: Be sure to support the board directly around the hole that a rivet is being removed from. Failure to do so could result in too much deflection and damage to the board.

4. Remove the heat sink assembly from the board.
5. Replace the processor by turning the screw on the socket to loosen the processor.

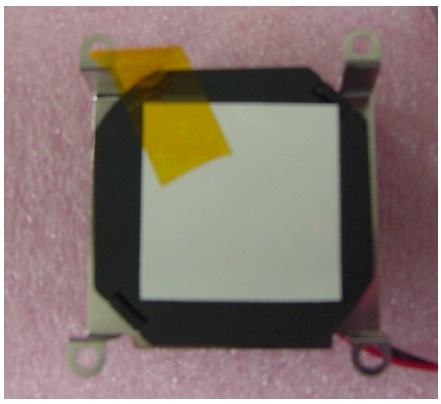
Note: Before replacing the heat sink assembly, it is very important to remove all thermal interface material (TIM) from the heat sink and processor. Be sure to clean the heat sink surface and surface of the die with isopropyl alcohol before re-installation.

6. Place the attachment shroud over the heat sink, as shown in Figure 4.

Figure 4. Top View of the Heat Sink

7. Turn the heat sink over so that the bottom is facing up.
8. Remove the protective liner from one side of the thermal interface material. It should come off fairly easy from the strips.
9. Place the protective liner on the bottom of the heat sink with ‘rolling finger pressure.’
10. Remove the remaining protective liner. To remove the protective liner, place a piece of tape at one corner (as shown in Figure 5) and pull up at a 180-degree angle.

Figure 5. Bottom View of Heat Sink



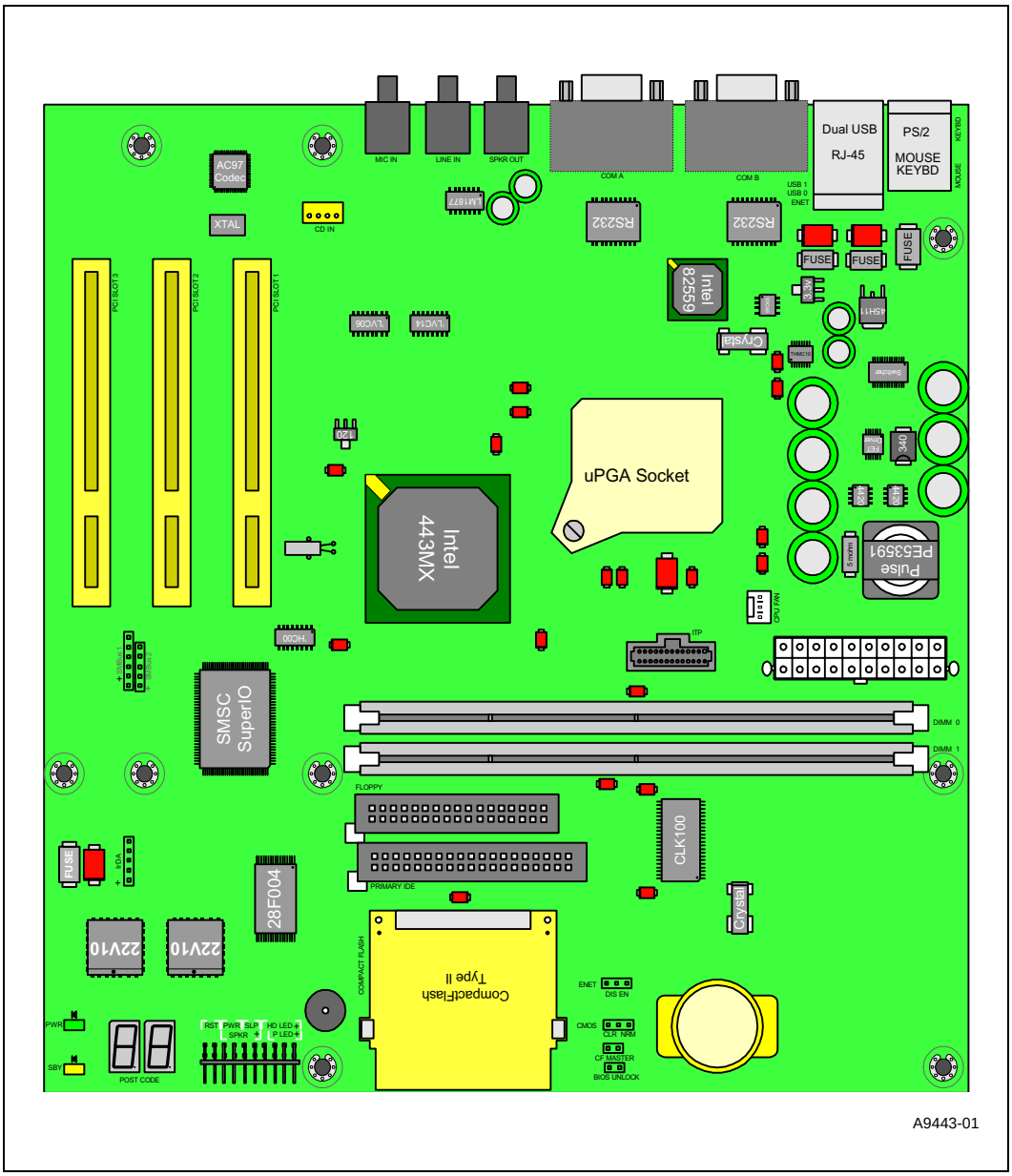
11. Place the heat sink on top of the die, making sure to align the holes in the shroud with those on the board.
12. Place the body of the rivet through the hole in the attach shroud. Ensure the spring is on the body and above the tab on the shroud.
13. Push the body through the hole in board. It is easiest to insert the rivet using a mechanical pencil or some other object that will allow you to push with even pressure. Be sure to insert the rivets in opposite corners, so even pressure on the die is maintained.

Warning: Be sure to support the board directly around the hole that a rivet is being inserted into. Failure to do so could result in too much deflection and could damage the board.

14. After all rivet bodies are inserted into the board, push the pins all the way into the body. It should look like Figure 3.
15. Plug the fan cable into the ATX power supply.

4.2 Connector Pinouts

Figure 6. Baseboard Layout Diagram



4.2.1 ATX Power Connector

Table 2 lists the signals assigned to the ATX style power connector.

Table 2. Power Connector (ATXPR1)

Pin	Name	Function
1	3.3 V	3.3 V
2	3.3 V	3.3 V
3	GND	Ground
4	+5V	+5 V VCC
5	GND	Ground
6	+5 V	+5 V VCC
7	GND	Ground
8	PWRGD	Power Good
9	5 VSB	Standby 5 V
10	+12 V	+12 V
11	3.3 V	3.3 V
12	-12 V	-12 V
13	GND	Ground
14	PS_ON#	Soft-off control
15	GND	Ground
16	GND	Ground
17	GND	Ground
18	-5 V	-5 V
19	+5 V	+5 V VCC
20	+5 V	+5 V VCC

4.2.2 Dual Stacked USB Connector

Table 3 lists the signals assigned to the dual stacked USB connector (USB1).

Table 3. USB Connector Pinout (USB1)

Pin	Signal Name
1,5	Power (fused)
2,6	USBP0# [USBP1#]
3,7	USBP0 [USBP1]
4,8	GND

4.2.3 PS/2-Style Mouse and Keyboard Connectors

Table 4 lists the signals assigned to the keyboard and mouse connector (U1). The mouse port is on the top and the keyboard port is on the bottom.

Table 4. PS/2-Style Mouse and Keyboard Pinout (U1)

Pin	Signal Name
1	Data
2	No Connect
3	GND
4	+5 V (fused)
5	Clock
6	No Connect

4.2.4 Serial Ports

Table 5 lists the signals assigned to the serial port connectors (COM1 and COM2).

Table 5. Serial Port Connector Pinout (COM1 and COM2)

Pin	Signal Name
1	DCD
2	Serial In (SIN)
3	Serial Out (SOUT)
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

4.2.5 Audio Connectors

Refer to Figure 2 on page 24 for the connectors referenced in this section.

Table 6 lists the signals assigned to the audio line-out connector.

Table 6. Audio Line-Out Connector Pinouts

Pin	Signal Name
Sleeve	GND
Tip	Audio Left Out
Ring	Audio Right Out

Table 7 lists the signals assigned to the audio line-in connector.

Table 7. Audio Line-In Connector Pinouts

Pin	Signal Name
Sleeve	GND
Tip	Audio Left In
Ring	Audio Right In

Table 8 lists the signal assigned to the audio mic-in connector.

Table 8. Audio Mic-In Connector Pinouts

Pin	Signal Name
Sleeve	GND
Tip	Mono In
Ring	Mic bias voltage

4.2.6 Compact Flash Connector

Table 9. Compact Flash Connector (Sheet 1 of 2)

Pin	Signal Name	Pin	Signal Name
1	Ground	26	Ground
2	Host Data 3	27	Host Data 11
3	Host Data 4	28	Host Data 12
4	Host Data 5	29	Host Data 13
5	Host Data 6	30	Host Data 14
6	Host Data 7	31	Host Data 15
7	IDEPDCS1#	32	IDEPDCS3#
8	Ground	33	N/C

Table 9. Compact Flash Connector (Sheet 2 of 2)

9	Ground	34	IDEPDIOR#
10	Ground	35	IDEPDIOW#
11	Ground	36	VCC
12	Ground	37	IDEPDIRQ
13	VCC	38	VCC
14	Ground	39	IDEPCSEL1#
15	Ground	40	N/C
16	Ground	41	IDERST#
17	Ground	42	IDEPDIORDY
18	Addr 2	43	N/C
19	Addr 1	44	VCC
20	Addr 0	45	IDEPDASP#
21	Host Data 0	46	IDEPDIAG#
22	Host Data 1	47	Host Data 8
23	Host Data 2	48	Host Data 9
24	IDEIOCS16#	49	Host Data 10
25	Ground	50	Ground

4.2.7 IDE Connector

Table 10 lists the signals assigned to the IDE connectors (IDE1 and IDE2).

Table 10. IDE Connector Pinouts for IDE1 and IDE2 (Sheet 1 of 2)

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	21	DRQ3
2	Ground	22	Ground
3	Host Data 7	23	I/O Write#
4	Host Data 8	24	Ground
5	Host Data 6	25	I/O Read#
6	Host Data 9	26	Ground
7	Host Data 5	27	IOCHRDY
8	Host Data 10	28	Ground
9	Host Data 4	29	DACK3#
10	Host Data 11	30	Ground
11	Host Data 3	31	IRQ14
12	Host Data 12	32	IOCS16#
13	Host Data 2	33	Addr1
14	Host Data 13	34	PDIAG
15	Host Data 1	35	Addr 0

Table 10. IDE Connector Pinouts for IDE1 and IDE2 (Sheet 2 of 2)

Pin	Signal Name	Pin	Signal Name
16	Host Data 14	36	Addr 2
17	Host Data 0	37	Chip Select 0#
18	Host Data 15	38	Chip Select 1#
19	Ground	39	Activity
20	N/C	40	Ground

4.2.8 Floppy Drive Connector

Table 11 lists the signals assigned to the floppy drive connector (FDC1).

Table 11. Floppy Drive Connector Pinouts (FDC1)

Pin	Signal Name	Pin	Signal Name
1	Ground	2	DRVDENO
3	Ground	4	Reserved
5	N/C	6	DRVDEN1
7	Ground	8	Index
9	Ground	10	Motor Enable A#
11	Ground	12	Drive Select B#
13	Ground	14	Drive Select A#
15	Ground	16	Motor Enable B#
17	Ground	18	DIR#
19	Ground	20	STEP#
21	Ground	22	Write Data#
23	Ground	24	Write Gate#
25	Ground	26	Track 00#
27	Ground	28	Write Protect#
29	N/C	30	Read Data#
31	Ground	32	Side 1 Select#
33	N/C	34	Diskette Change#

4.2.9 32-Bit PCI Slot Connector

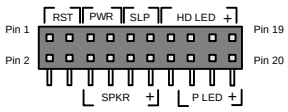
Table 12 lists the signals assigned to the 32-Bit PCI slot connectors (PCI1, PCI2, and PCI3).

Table 12. 32-Bit PCI Slot Connector Pinouts

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A01	GND	B01	-12 V	A32	AD16	B32	AD17
A02	+ 12 V	B02	GND	A33	3.3 V	B33	CBE2#
A03	VCC	B03	GND	A34	FRAME#	B34	GND
A04	VCC	B04	No Connect	A35	GND	B35	IRDY#
A05	VCC	B05	VCC	A36	TRDY#	B36	3.3 V
A06	PIRQ1#	B06	VCC	A37	GND	B37	DEVSEL#
A07	PIRQ3#	B07	PIRQ2#	A38	STOP#	B38	GND
A08	VCC	B08	PIRQ0	A39	3.3 V	B39	LOCK#
A09	No Connect	B9	PRSNT1B #	A40	SDONE	B40	PERR#
A10	VCC	B10	No Connect	A41	SBO#	B41	3.3V
A11	No Connect	B11	PRSNT2B #	A42	GND	B42	SERR#
A12	GND	B12	GND	A43	PAR	B43	3.3 V
A13	GND	B13	GND	A44	AD15	B44	CBE1#
A14	No Connect	B14	No Connect	A45	3.3V	B45	AD14
A15	RST#	B15	GND	A46	AD13	B46	GND
A16	VCC	B16	PCLK3	A47	AD11	B47	AD12
A17	GNT1#	B17	GND	A48	GND	B48	AD10
A18	GND	B18	REQ#	A49	AD9	B49	GND
A19	PPME#	B19	VCC	A50	KEY	B50	KEY
A20	AD30	B20	AD31	A51	KEY	B51	KEY
A21	3.3 V	B21	AD29	C52	CBEO#	D52	AD8
A22	AD28	B22	GND	C3	3.3 V	D53	AD7
A23	AD26	B23	AD27	C54	AD6	D54	3.3 V
A24	GND	B24	AD25	C55	AD4	D55	AD5
A25	AD24	B25	3.3 V	C56	GND	D56	AD3
A26	IDSEL	B26	CBE3#	C57	AD2	D57	GND
A27	3.3 V	B27	AD23	C58	AD0	D58	AD1
A28	AD22	B28	GND	C59	VCC	D59	VCC
A29	AD20	B29	AD21	C60	N/C	D60	ACK64#
A30	GND	B30	AD19	C61	VCC	D61	VCC
A31	AD18	B31	3.3 V	C62	VCC	D62	VCC

4.3 Jumpers

Front Panel Connector



FRONT VIEW

1	RESET BUTTON (GND)	2	RESET BUTTON (NON-RESUME)
3	RESET BUTTON (RESUME WELL)	4	ONBOARD SPEAKER IN (-)
5	POWER BUTTON	6	SPEAKER (-)
7	POWER BUTTON	8	GND
9	SLEEP BUTTON	10	N.C.
11	SLEEP BUTTON	12	SPEAKER (+)
13	N.C.	14	N.C.
15	N.C.	16	POWER LED (-)
17	HD LED (-)	18	N.C.
19	HD LED (+)	20	POWER LED (+)

NOTES:
1. Normal RESET should connect between pins 1 and 3. Alternate reset connects between 1 and 2, but RESUME well will not be reset in this case.
2. Onboard speaker is enabled with a jumper on pins 4 and 6. To use an external speaker, remove jumper and connect cable to pins 6, 8, 10, and 12.

4.3.1 CMOS Jumper

The CMOS jumper controls the power to the battery backed-up CMOS memory. This CMOS memory stores system information required by the BIOS during startup. For normal operation, jumper pins 1 and 2. To clear the CMOS RAM, perform the following steps:

1. Shut down the system.
2. Disconnect the power supply (ATXPR1).
3. Remove jumper from pins 21 and 22. Short pins 20 and 21 (clear CMOS).
4. Wait 10 seconds.
5. Replace the jumper on pins 21 and 22 (normal operation).
6. Reconnect the power supply (ATXPR1).
7. Boot the system and enter the BIOS setup screen to reconfigure the system.

Short Pins 21 and 22	Normal Operation (default)
Short Pins 20 and 21	Clear saved CMOS data

4.3.2 ENET Jumper

When using the Ethernet controller you must short pins 18 and 19 on the ENET jumper. To deactivate, short pins 17 and 18.

4.3.3 CF MASTER Jumper

To make the compact flash the IDE master, short pins 23 and 24.

4.3.4 BIOS UNLOCK Jumper

You can choose to lock access to the BIOS by shorting 25 and 26.

BIOS Quick Reference 5

The evaluation board is licensed with a single copy of Embedded BIOS and Embedded DOS software from General Software, Inc. This software is provided for demonstration purposes only and must be licensed directly from General Software, Inc. for integration with new designs. General Software may be reached at (800) 850-5755, on the Web at http://www.gensw.com, or via e-mail at sales@gensw.com.

BIOS updates may periodically be posted to the Intel Developers' Web site at http://developer.intel.com/.

5.1 Embedded BIOS Introduction

General Software's Embedded BIOS brand BIOS (Basic Input/Output System) pre-boot firmware is the industry's standard product used by most designers of embedded x86 computer equipment in the world today. Its superior combination of configurability and functionality enables it to satisfy the most demanding ROM BIOS needs for embedded designers. Its modular architecture and high degree of configurability make it the most flexible BIOS in the world.

Although Embedded BIOS can be made to behave like a PC BIOS, it has a fundamentally different role. The goal of a PC BIOS is to provide the same standard user experience for all the systems it runs on. For example, this allows a wide range of users to intuitively use any notebook computer, regardless of brand. The goal of Embedded BIOS is completely different—it allows the embedded equipment manufacturer to differentiate its product from competing products in a way that is quick and cost effective—allowing the manufacturer to pass savings on to the end user.

This operating guide describes all of the possible user features of Embedded BIOS. Most of these features are included in the demonstration BIOS on this platform, but not all can be included, either due to space limitations or because features have conflicting requirements. Some features require hardware support that is not present in all designs. You can see a list of included and available features in the BIOS browser included in your demonstration BIOS. Instructions for accessing the BIOS Browser are found later in this guide.

Once you move from the demonstration BIOS to your own custom adaptation, you may choose to incorporate some or all applicable features, modifying them as necessary to fit your application. Therefore, some of the features discussed in this operating guide may not apply to your system's Demonstration BIOS.

5.1.1 Features

Dedicated to the embedded 80x86-based market, Embedded BIOS offers special-purpose features not provided by typical PC BIOS implementations.

Embedded BIOS's CPU-specific personality modules allow support of high-integration processors that have on-board timers, DMA controllers, serial ports, watchdog timers, power management, and other features.

With chipset support, virtually any add-on chipset, or CPU with on-board chipset can be supported by Embedded BIOS. Traditionally, chipsets provide DRAM memory management, bus control, and address space management. The Embedded BIOS architecture provides for chipset personality modules that can be selected for a project.

Embedded BIOS's board-level support provides for the OEM to control the BIOS's access to chipset and CPU modules in major or subtle ways. Essentially a routing module, the board module contains routines, which call associated routines in the chipset and CPU personality modules. The board module routines can be modified as needed to replace the calls to the underlying CPU and chipset modules with custom code, as needed for hardware designs that work differently than standard reference designs supported by General Software.

Embedded BIOS is implemented in hand-optimized 80x86 assembly language, with special code paths for many generations of processors. The code paths have been hand-tuned to minimize the interrupt latency commonly found in desktop BIOS implementations, and many of the "hot paths" of the BIOS have been straight-line optimized for the common case.

ROM disk software is integrated directly with the system BIOS itself, eliminating the need to populate the ROM scan area with ROM BIOS extensions to simulate one or more floppy or hard disks in ROM. Instead, with the ROM disk configuration feature enabled, an image of a floppy or hard disk can be stored in ROM anywhere in the address space of the TARGET and treated as a solid-state drive. If the ROM disk feature is enabled, the ROM disk can be selectively turned on or off in the setup screen.

RAM disk software is also integrated directly into the system BIOS to support PCMCIA SRAM cards and other RAM areas as floppy or hard disk emulators. SETUP even has a formatting screen for the RAM disk.

The system BIOS supports a Resident Flash Disk (RFD) that provides read/write access to sectored Flash devices as though they were a floppy or hard disk of up to 32 Mbytes in size. The inclusion of this software makes it easy to support Flash in embedded and hand-held consumer electronics. Multiple RFDs can be supported in the same TARGET.

The integrated BIOS debugger gives the engineer bringing up new hardware the capability of debugging the hardware with powerful tools like a disassembler, breakpoints, CMOS editing, A20-line gating commands, cache control commands, PCI bus management commands, and Super I/O controls. The debugger is very useful for debugging chipset modules, CPU class modules, and initialization of user ROM extensions and hardware. Like the setup screen, the integrated BIOS debugger can run directly on a PC keyboard and video screen, or it can be redirected over an RS-232 serial link.

Embedded systems deployed into more inaccessible areas need watchdog timer support, so that they can automatically restart in the event that application or system software fails. Embedded BIOS provides watchdog timer control functions to allow operating systems and application programs to use watchdog timer hardware found in chipsets and certain CPU classes.

Keyboard and video output may be selectively redirected over RS-232 serial links for different system components. For example, standard console I/O, such as that used by DOS and DOS applications, can be redirected over any COM port, including those built-into high-integration CPUs. Debugger I/O and setup screen I/O can also be redirected over the same or different RS-232 serial links.

A special Manufacturing Mode feature provides the necessary provisions for programming electronics products through a high-speed serial link, and then testing and repairing the same items in the field at service centers. The OEM can write custom software that uses Embedded BIOS Manufacturing Mode functions to perform virtually any maintenance or programming task on the TARGET under host control.

5.1.2 PC BIOS Features

Embedded BIOS provides a comprehensive Power-On Self-Test (POST) algorithm that is automatically configured for the peripherals and capabilities selected by the adaptation engineer. During POST, hardware is initialized and tested, including the CPU, RAM, and peripherals. POST provides beep code diagnostics for errors when a display is not available, as well as error message diagnostics on the display when available. POST can also be configured to output status report codes to a manufacturing port (typically, port 80h) so that automated Q/A equipment can determine the status of a system during POST. A special set of ASCII POST status codes are also available through a serial port, for flexibility in the debugging process when new hardware is being brought up. Either POST code system, or both, can be used during debugging.

The Embedded BIOS SETUP screen system is configurable at the source level by the adaptation engineer to contain any combination of subscreens, including basic CMOS configuration, custom configuration, shadow configuration, diagnostics screens, manufacturing mode, debugger access, and formatting of drive emulators such as RAM and RFD drives. Setup screens can also be customized at the source level (in the board personality module) to contain custom fields as required by the application.

The BIOS browser is also available for your use. Selectable as a boot action or from within setup, it can present HTML files to your end users to document the platform, provide contact information for your company, etc. This provides a convenient means of providing information to help users recover from hardware problems, like a failed hard drive.

Also available is a password protection system, so that a password must be provided by the end-user before POST allows booting of an operating system. The password is stored in CMOS, is one-way encrypted, and can be modified in a setup screen.

The ability to shadow slower ROM devices with DRAM or SRAM is selectable in the shadow setup screen and calls chipset-specific code to enable shadowing for the BIOS ROM itself or for feature ROMs on a 16 Kbyte region basis. DRAM may take the form of FP, EDO, SDRAM, RDRAM, or other technologies.

Embedded BIOS provides extensive support for both internal CPU cache control (i486 and above) and external cache control (typically chipset-controlled). Internal cache is managed by the CPU class personality modules, whereas external cache is managed by the cache manager, which directs peripherals (chipset, 8042, custom I/O ports, or CPU integrated peripherals) to manage the cache. Keyboard controls on the PC/AT keyboard are implemented for enabling and disabling the cache on the fly (while the system is running). The BIOS provides cache control services to applications that allow operating systems and user code to control and inspect the status of the cache.

CPU speed controls are handled by the system BIOS by routing control through the appropriate logic (chipset, 8042, custom I/O ports, or CPU integrated peripherals). As with cache control, CPU speed is controllable while the system is running at the keyboard or via programming interfaces.

5.1.3 Software Compatibility

Embedded BIOS offers a high degree of compatibility with past and current BIOS standards, allowing it to run off-the-shelf operating system software and application software.

Embedded BIOS has been tested with all industry-standard operating systems, including versions of Windows, Linux, DOS, and real time operating systems.

Embedded BIOS is rigorously tested with programs such as AMI Diag, MSD, Check-It, Manifest, Q/A Plus, ensuring its compatibility with established desktop application standards.

In addition to its standard data structures and programming interfaces, Embedded BIOS provides support for industry-standard initiatives, including ACPI, APM, El Torito, Legacy USB, MP, PCI, PMM, PXE, and SMBIOS (formerly DMI).

5.2 Power On Self Test

When the TARGET is powered on, Embedded BIOS tests and initializes the hardware and programs the chipset and other peripheral components. During this time, Power On Self Test (POST) progress codes are written by the system BIOS to I/O port 80h, allowing the user to monitor the progress with a special monitor. Section 5.7.1, “Embedded BIOS POST Codes” on page 57 lists the POST codes and their meanings.

During early POST, no video is available to display error messages should a critical error be encountered; therefore, POST uses beeps on the speaker to indicate the failure of a critical system component during this time. Consult Section 5.8, “Critical Error Beep Codes” on page 60 for a list of beep codes used by the TARGET’s BIOS.

5.2.1 The BIOS User Interface

The TARGET BIOS can use the standard keyboard and video device, or use console redirection to demonstrate headless operation. For headless operation, remove the standard keyboard and screen devices and the system will boot unattended. If an RS232 cable is attached to COM1, a PC/AT-style character-based POST is available from HyperTerminal, PROCOMM, or any other terminal emulator software that supports VT100 emulation.

When a keyboard and video device are attached, the TARGET can display either a traditional character-based PC BIOS display with memory count-up, or it can display a graphical POST with splash screen and progress icons. Both POST displays accept a <DEL> key press to enter the setup screen, and both display boot-time progress activity displays. The graphical display shows the status of file system devices and even OEM-defined devices (when the OEM adapts the BIOS to a particular OEM platform), but omits character-based PCI resource display. The text-based POST displays the memory count-up and the PCI resource assignment table.

Figure 7 shows the format of the text-based POST display. The display is very similar if console redirection through a COM port is used instead.

Figure 7. BIOS POST, the Text-based System

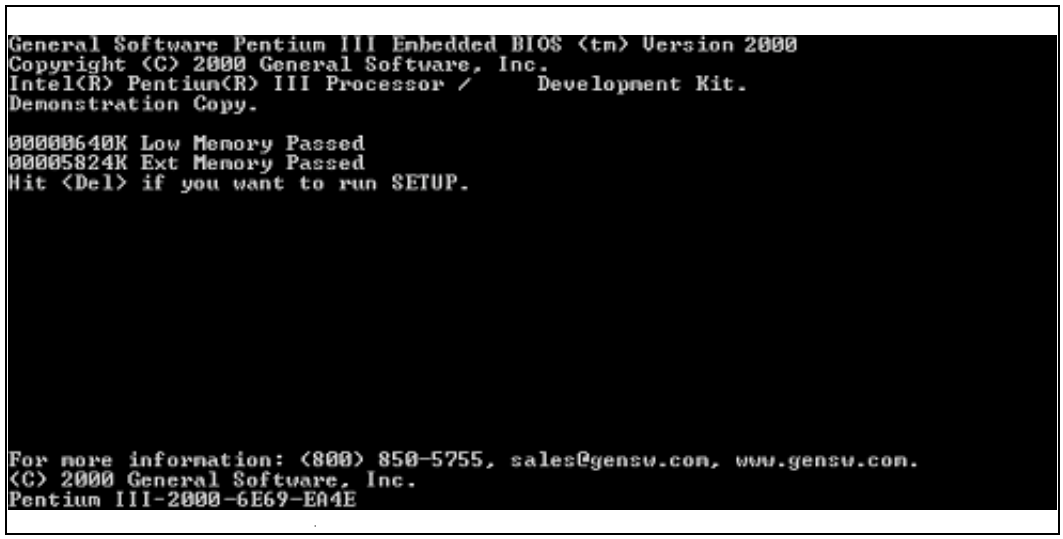
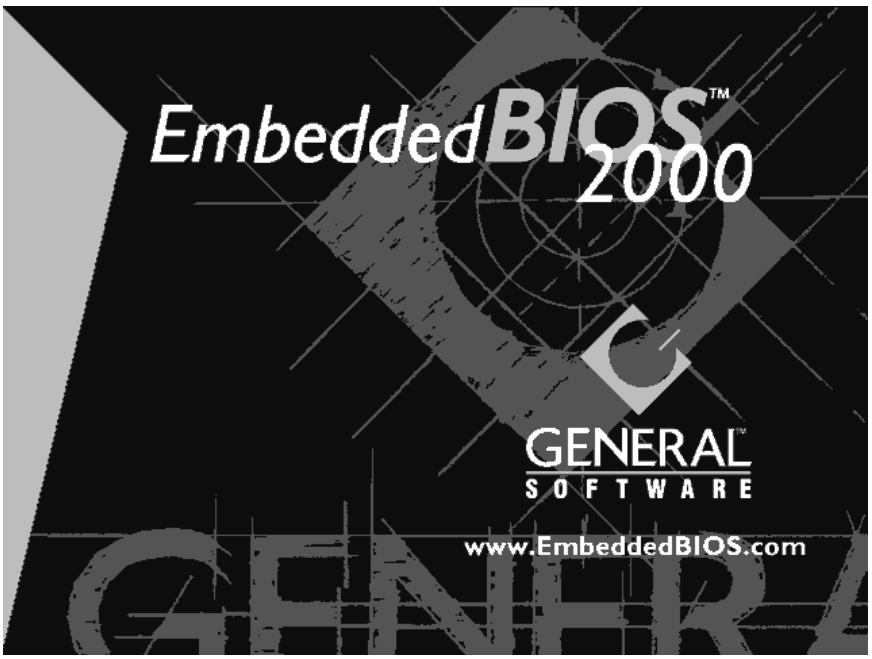


Figure 8 shows the graphical version of POST. The BIOS decompresses the main image, and can display multiple overlaid graphics at various points in POST. The OEM can define the entire sequence and control the timing of the system for an embedded application, and can arrange to have different graphics displayed on each successive boot of the system. This feature is ideal for embedded systems that must show evidence of operation during startup, while the application loads underneath the splash screen. Once the application begins writing to the screen, the splash screen relinquishes control, providing a seamless graphical progression for the end user.

Figure 8. The Graphical POST



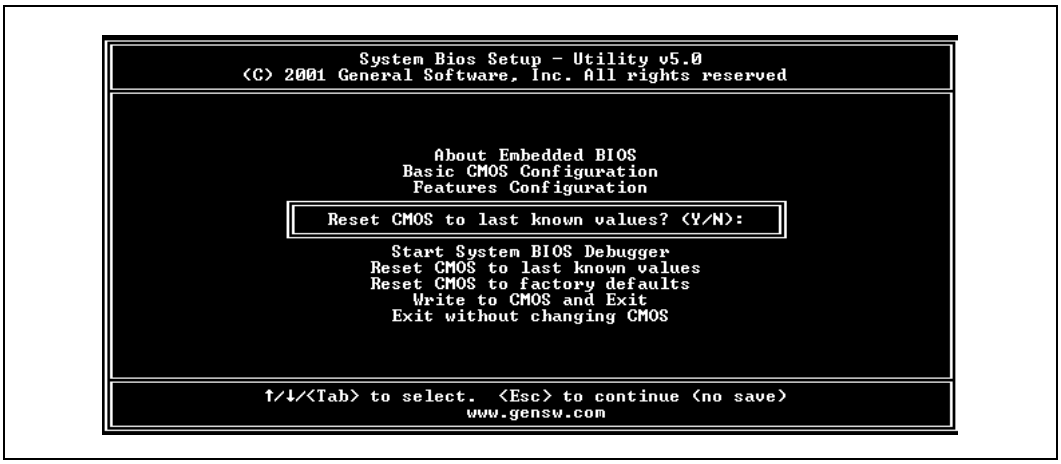
When the TARGET is powered on for the first time, you'll need to configure the system through the Setup Screen System (described later) before peripherals, such as disk drives, are recognized by the BIOS. The information is written to battery-backed CMOS RAM on the board's Real Time Clock. Should the board's battery fail, this information will be lost and the board will need to be reconfigured.

The TARGET's Basic Setup Screen provides an option to disable the graphical POST and switch to the legacy text-based version. This feature may not permanently disable the graphical POST if the BIOS adaptation calls for reverting to the graphical form after so many boots. If you find that the graphical POST comes back after several boots, it is because this option is enabled for this platform. Naturally, the OEM can use the Embedded BIOS Adaptation Kit to control whether Setup can be used to dictate the policy, and whether it is permanent or temporary.

5.3 Setup Screen System

The TARGET is configured from within the Setup Screen System, a series of menus that can be invoked from POST by pressing the <DEL> key if the main keyboard is being used, or by pressing Ctrl C (^C) if the console is being redirected to a terminal program.

Figure 9. Embedded BIOS Setup Screen Menu

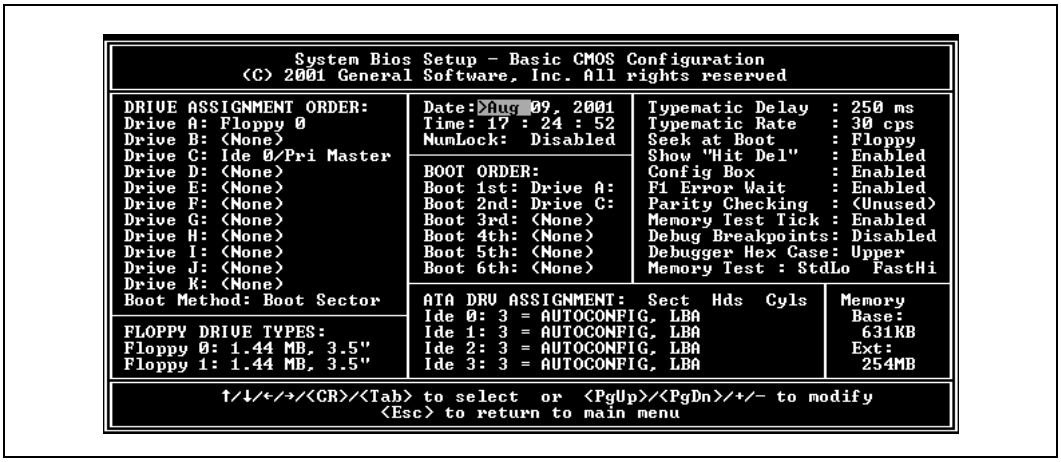


Once in the Setup Screen System (Figure 9), the user can navigate with the UP and DOWN arrow keys from the main console or use the Ctrl E (^E) and Ctrl X (^X) keys from the remote terminal program to accomplish the same thing. TAB and ENTER are used to advance to the next field, and '+' and '-' keys cycle through values, such as those in the Basic Setup Screen or the Diagnostics Setup Screen.

5.3.1 Basic CMOS Configuration Screen

The TARGET's drive types, boot activities, and POST optimizations are configured from the Basic Setup Screen (Figure 10). To use disk drives with your system, you must select appropriate assignments of drive types in the left-hand column. Then, if you are using true floppy and IDE drives (not memory disks that emulate these drives), you need to configure the drive types themselves in the Floppy Drive Types and IDE Drive Geometry sections. Finally, you'll need to configure the boot sequence in the middle of the screen. Once these selections have been made, your system is ready to use.

Figure 10. Embedded BIOS Basic Setup Screen



5.3.2 Configuring Drive Assignments

Embedded BIOS allows the user to map a different file system to each drive letter. The BIOS allows file systems for each floppy (Floppy0 and Floppy1), each IDE drive (Ide0, Ide1, Ide2, and Ide3), and memory disks when configured (Flash0, ROM0, RAM0, etc.). Figure 10 shows how the first floppy drive (Floppy0) is assigned to drive A: in the system, and then shows how the first IDE drive (Ide0) is assigned to drive C: in the system.

To switch two floppy disks around or two hard disks around, map Floppy0 to B: and Floppy1 to A:, and for hard disks map Ide0 to D: and Ide1 to C:.

Caution: Take care to not skip drive A: when making floppy disk assignments, as well as drive C: when making hard disk assignments. The first floppy should be A:, and the first hard drive should be C:. Also, do not assign the same file system to more than one drive letter. Thus, Floppy0 should not be used for both A: and B:. The BIOS permits this to allow embedded devices to alias drives, but desktop operating systems may not be able to maintain cache coherency with such a mapping in place.

A special field in this section entitled “Boot Method: (Windows CE/Boot Sector)” is used to configure the CE Ready feature of the BIOS. For normal booting (DOS, Windows NT, etc.), select “Boot Sector” or “Unused.”

5.3.3 Configuring Floppy Drive Types

If true floppy drive file systems (and not their emulators, such as ROM, RAM, or Flash disks) are mapped to drive letters, then the floppy drives themselves must be configured in this section. Floppy0 refers to the first floppy disk drive on the drive ribbon cable (normally drive A:), and Floppy1 refers to the second drive (drive B:).

5.3.4 Configuring IDE Drive Types

If true IDE disk file systems (and not their emulators, such as ROM, RAM, or Flash disks) are mapped to drive letters, then the IDE drives themselves must be configured in this section. The following table shows the drive assignments for Ide0-Ide3:

File System Name	Controller	Master/ Slave
Ide0	Primary (1f0h)	Master
Ide1	Primary (1f0h)	Slave
Ide2	Secondary (170h)	Master
Ide3	Secondary (170h)	Slave

To use the primary master IDE drive in your system (the typical case), configure Ide0 in this section, and map Ide0 to drive C: in the Configuring Drive Assignments section.

The IDE Drive Types section lets you select the type for each of the four IDE drives: None, User, Physical, LBA, or CHS.

The **User** type allows the user to select the maximum cylinders, heads, and sectors per track associated with the IDE drive. This method is now rarely used since LBA is now in common use.

The **Physical** type instructs the BIOS to query the drive's geometry from the controller on each POST. No translation on the drive's geometry is performed, so this type is limited to drives of 512 Mbytes or less. Commonly, this is used with embedded ATA PC cards.

The **LBA** type instructs the BIOS to query the drive's geometry from the controller on each POST, but then translate the geometry according to the industry-standard LBA convention. This supports up to 128 Gbyte drives. ***Use this method for all new drives.***

The **CHS** type instructs the BIOS to query the drive's geometry from the controller on each POST, but then translate the geometry according to the Phoenix CHS convention. Using this type on a drive previously formatted with LBA or physical geometry might show data as being missing or corrupted.

EMBEDDED BIOS supports user-defined steps in the boot sequence. When the entire system has been initialized, POST executes these steps in order until an operating system successfully loads. In addition, other pre-boot features can be run before, after, or between operating system load attempts. The following actions are supported:

- Drive A: - D:

  Boot operating system from specified drive. If "Loader" is set to "BootRecord" or "Unused," then the standard boot record will be invoked, causing DOS, Windows95, Windows 98, Windows ME, Windows 2000, Windows NT, Windows XP, Linux, or other industry-standard operating systems to load. If "Boot Method" is set to "Windows CE", then the boot drive's boot record will not be used, and instead the BIOS will attempt to load and execute the Windows CE Kernel file, NK.BIN, from the root directory of each boot device.

- CDROM

Boot from the first IDE CDROM found that contains an El Torito bootable CDROM.

- Debugger

  Launch the Integrated BIOS Debugger. To return exit the debugger environment, type “G” at the debugger prompt and press ENTER.

- MFGMODE

  Initiate Manufacturing Mode, allowing the system to be configured remotely via an RS232 connection to a host computer.

- WindowsCE

  Execute a ROM-resident copy of Windows CE, if available. This feature is not applicable unless configured by the OEM in the BIOS adaptation.

- DOS in ROM

  Execute a ROM-resident copy of DOS, if available. This feature is not applicable unless an XIP copy of DOS has been stored in the BIOS boot ROM.

- Alarm

  Generate an alarm by beeping the speaker and sending a signal to a Firmware Application running in the firmbase environment. The application can perform whatever processing is necessary to handle the alarm, including taking local action, interacting with other tightly coupled computers, or even notifying other systems on the network, for example. These applications are beyond the scope of the Embedded BIOS Adaptation Kit.

- Maintenance

  Enter maintenance mode by sending a signal to a firmware application running in the firmbase environment. The application can perform whatever processing is necessary to implement the maintenance mode, which is largely defined to mean some state where the system is capable of being diagnosed and/or repaired in the field. These applications are beyond the scope of the Embedded BIOS Adaptation Kit.

- RAS

  Enter remote access mode by sending a signal to a firmware application running in the firmbase environment. The application can perform whatever processing is necessary to implement the RAS mode, which is largely defined to mean some state where the system accepts remote connections for normal operation; not specifically for field maintenance. These applications are beyond the scope of the Embedded BIOS Adaptation Kit.

- Power Off

  Cause the TARGET to switch off its power with a “soft off” feature, and signal firmware applications running in the firmbase environment that power is going down. These applications are beyond the scope of the Embedded BIOS Adaptation Kit.

- Reboot

  Reboot the TARGET, and send a signal to a Firmware Application running in the Firmbase environment indicating that the TARGET is rebooting. These applications are beyond the scope of the Embedded BIOS Adaptation Kit.

- CLI

  Enter command line mode by calling a special Board Module Function (BoardPostControl) that can be used to implement an OEM-defined Command Language Interpreter. The design of such an interpreter is beyond the scope of the Embedded BIOS Adaptation Kit.

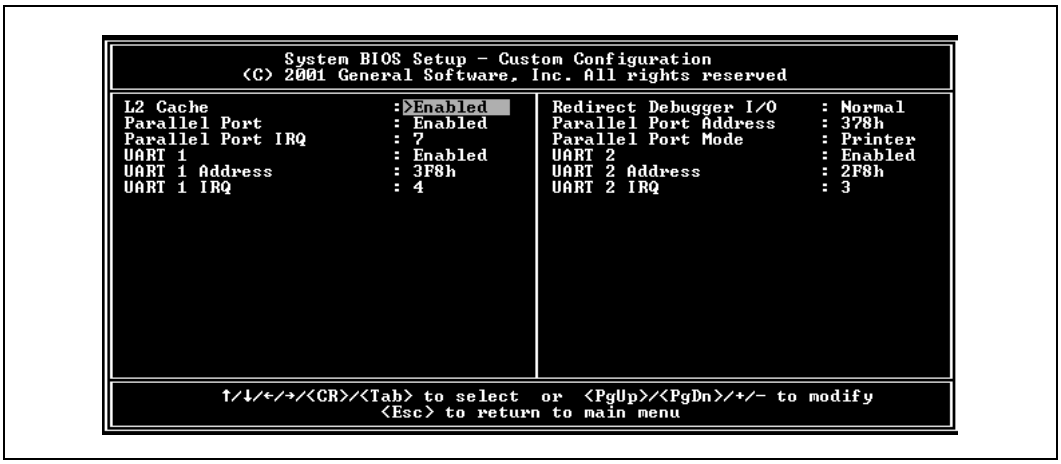
- None

No action; POST proceeds to the next activity in the sequence.

5.3.5 Custom Configuration Setup Screen

The TARGET's hardware-specific features are configured with the Custom Setup Screen (Figure 11). All features are straightforward except for the Redirect Debugger I/O option, which is an extra embedded feature that allows the user to select whether the Integrated BIOS Debugger should use standard keyboard and video or RS232 console redirection for interaction with the user. If no video is available, the debugger is always redirected.

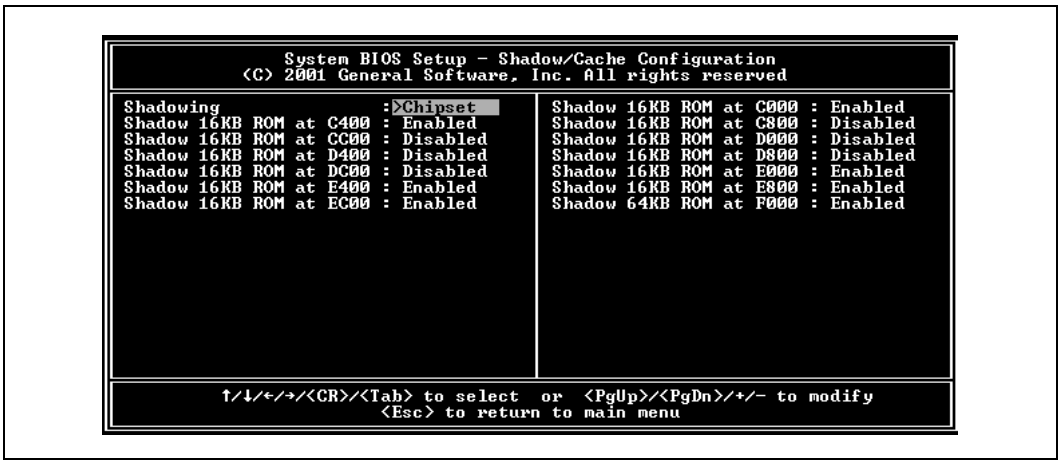
Figure 11. Embedded BIOS Custom Setup Screen



5.3.6 Shadow Configuration Setup Screen

The TARGET's Shadow Configuration Setup Screen (Figure 12) allows the selective enabling and disabling of shadowing in 16 Kbyte sections, except for the top 64 Kbytes of the BIOS ROM, which is shadowed as a unit. Normally, shadowing should be enabled at C000/C400 (to enhance VGA ROM BIOS performance) and then E000-F000 should be shadowed to maximize system ROM BIOS performance.

Figure 12. Embedded BIOS Shadow Setup Screen

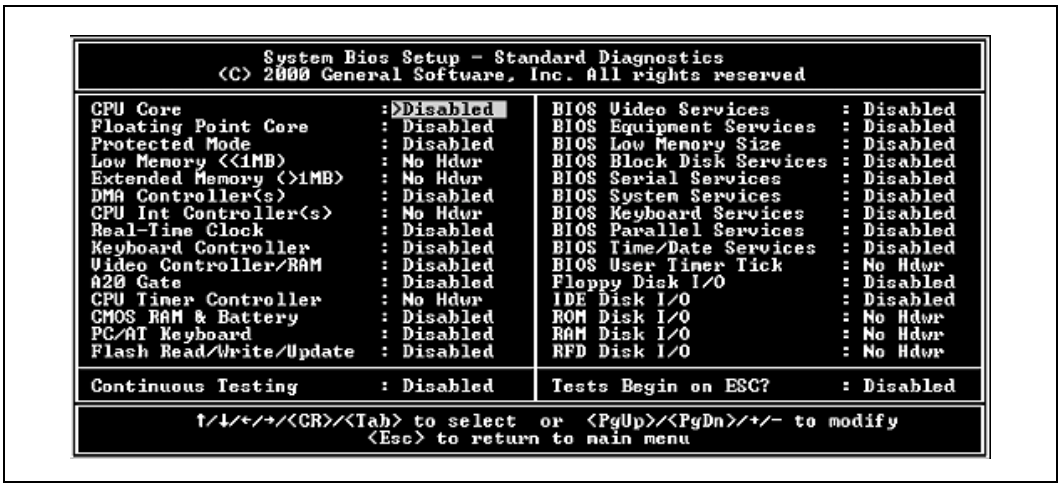


Embedded systems may require automated burn-in testing in the development cycle. This facility is provided directly in the TARGET's system BIOS through the Standard Diagnostics Routines Setup Screen (Figure 13). To use the system, selectively enable or disable features to be tested, and then enable the "Tests Begin on ESC?" option to cause the system test suite to be invoked. To repeat the system test battery continuously, you should also enable the "Continuous Testing" option. When continuous testing is started, the system will continue until an error is encountered.

Caution: The disk I/O diagnostics perform write operations on those drives; therefore, only spare drives should be used that do not contain data that could be harmed by the test.

Warning: The keyboard test may fail when in fact the hardware is operating within reasonable limits. This is because although the device may produce occasional errors, the BIOS retries operations when failures occur during normal operation of the system.

Figure 13. Standard Diagnostic Routines Setup Screen



5.3.7 Start System BIOS Debugger Setup Screen

The Embedded BIOS Integrated Debugger may be invoked from the Setup Screen main menu, as well as a boot activity. Once invoked, the debugger will display the debugger prompt:

EBDEBUG:

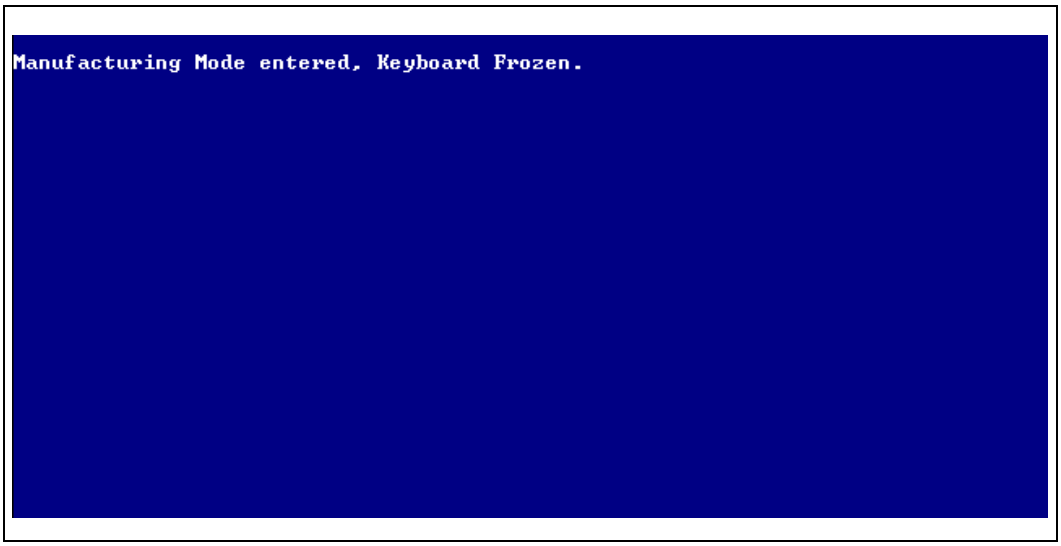
and await debugger commands. To resume back to the Setup Screen main menu, type the following command, which instructs the debugger to "go":

EBDEBUG: **G** (ENTER)

5.3.8 Start RS232 Manufacturing Link Setup Screen

The Embedded BIOS Manufacturing Mode may be invoked from the Setup Screen main menu, as well as a boot activity. Once invoked, Manufacturing Mode takes over the system and freezes the system console (Figure 14). The host can resume operation of the system and give control back to the TARGET Setup Screen system with special control software.

Figure 14. Start RS232 Manufacturing Link Setup Screen



5.3.9 Manufacturing Mode

The TARGET's BIOS may provide a special mode, called Manufacturing Mode, which allows the TARGET to be controlled by a host computer such as a laptop or desktop PC. Running special software supplied by General Software, the host can access the TARGET's drives and manage the file systems on the TARGET, reprogram Flash memories, and test the TARGET hardware.

There are several methods by which the TARGET can enter Manufacturing Mode. These methods are detailed elsewhere in this manual and others.

Once the TARGET has entered Manufacturing Mode, the host PC may cause the TARGET to perform functions by issuing commands in protocol over the RS-232 connection. There are two ways to access the TARGET from the host PC.

5.3.9.1 Sample Manufacturing Mode HOST Program

The first way is to run a program that accesses the host-side Manufacturing Mode functions. An example of such a program is `HOST.EXE`, which can be obtained from General Software. This program runs under DOS and, using a full-screen windowing interface, illustrates the basic functionality of the Manufacturing Mode protocol. It should be noted that this program is a working example program, and is not intended to be a production-quality control tool.

Run the HOST program on a "host" computer, so that its main menu is displayed. By default HOST connects via COM1 (3F8h). The default baud rate is set to "auto," meaning it will use whatever baud rate the TARGET is set to. You can change both of these by using command line switches. Type "HOST /?" for the available switches.

On the host, select "Get Target Attention," within a couple seconds of selecting the manufacturing mode on the TARGET. You should see the host program immediately display a yellow status box that shows that the connection has been established.

If the connection has not been established, try the connection again on the host side, or reboot the TARGET and try again, this time having the host program get the TARGET's attention within about two seconds of the TARGET's entering of manufacturing mode. If this still fails, check that your null modem serial cable is connected securely to the proper ports. You may also want to lower the baud rate for the manufacturing mode on the TARGET, since a higher baud rate may be more error prone.

Once you have established a connection, you can use HOST to test the link by continuously exercising it, or scanning the TARGET's drives, or uploading files in Flash, and more.

5.3.9.2 Manufacturing Mode Drive Redirection

The second way to access the TARGET through Manufacturing Mode is to install the `MFGDRV.SYS` device driver on the host system. This device driver loads under MS-DOS and Windows 98 DOS mode, and maps a new drive letter on the host to a drive on the TARGET. It is a DOS-only driver, and will not operate under Linux or Windows, not even in a Windows DOS box.

The INT 13h redirection support in the Manufacturing Mode protocol can be exposed by loading the `MFGDRV.SYS` device driver on the host by using the following `CONFIG.SYS` line:

```
DEVICE=MFGDRV.SYS /BAUD=rate /PORT=COMn /UNIT=u /AUTO
```

This device driver runs under any DOS-compatible operating system, and creates a drive letter on your host PC (usually D: if your last hard drive is C:) that can be used to interact with the specified INT 13h unit.

The *u* parameter specifies the BIOS unit number of the floppy disk, RAM disk, RFD drive, or ROM disk to be redirected, where 0 corresponds to drive A: and 1 for drive B. By default, this value is 80 (a hex number without a "0x" in front or 'h' appended to it), which corresponds with the unit for the first hard drive or emulator.

The `/BAUD=rate` parameter can be used to match the baud rate used by the TARGET's BIOS. Legal values are 19K, 28K, 38K, 56K, and 115K. If this parameter is not specified, then the baud rate is autodetected.

The `/AUTO` parameter, if specified, tells `MFGDRV.SYS` to automatically format the remote drive if it determines that it is unformatted. By default, `MFGDRV.SYS` will not automatically format the remote drive, and will instead examine the media for a pre-existing format. If not found, then `MFGDRV.SYS` asks the host PC operator if the remote drive should be formatted.

Once the connection is established, you can read and write the TARGET's drive as if it were simply another drive on your host system. The only difference is that it will be a bit slower over the serial connection.

Note: `MFGDRV.SYS` assumes that other software does not reprogram the COM port being used on the host for its purposes, and that it has exclusive access to it. If you run other software, such as terminal

emulation programs, they may disable the COM port UART, causing `MFGDRV.SYS` to appear to stop working. It is best to avoid running such software on the host when `MFGDRV.SYS` is loaded.

Note: `HOST.EXE` is an example of such a program, since it takes over the UART for its own purposes. If you run `HOST.EXE` when `MFGDRV.SYS` is loaded, you must reboot the host PC for the `MFGDRV.SYS` driver to reestablish its control over the UART.

A full discussion of the uses of Manufacturing Mode is beyond the scope of this manual. Complete documentation and host-side software are available directly from General Software. For more information, visit the General Software web site at www.gensw.com.

5.4 Console Redirection

The TARGET can operate either with a standard PC/AT or PS/2 keyboard and VGA video monitor, or with a special emulation of a console over an RS232 cable connected to a host computer running a terminal program. To see an example session with HYPERTERMINAL, see the debugger section's screen display.

To use the Console Redirection feature, remove the video display card from the system so that no video ROM is available for the BIOS to detect. In the absence of any video support, the BIOS automatically switches its keyboard and screen functions to serial I/O over COM1 on the board. The hardware connection to the host computer requires a null modem cable.

The software on the TARGET can be any terminal emulation program that supports ANSI terminal mode, using 9600 baud, no parity, and one stop bit (Note: This can be modified by the OEM during BIOS adaptation.) The program must be set to not use flow control, or the console may seem to stall or not accept input.

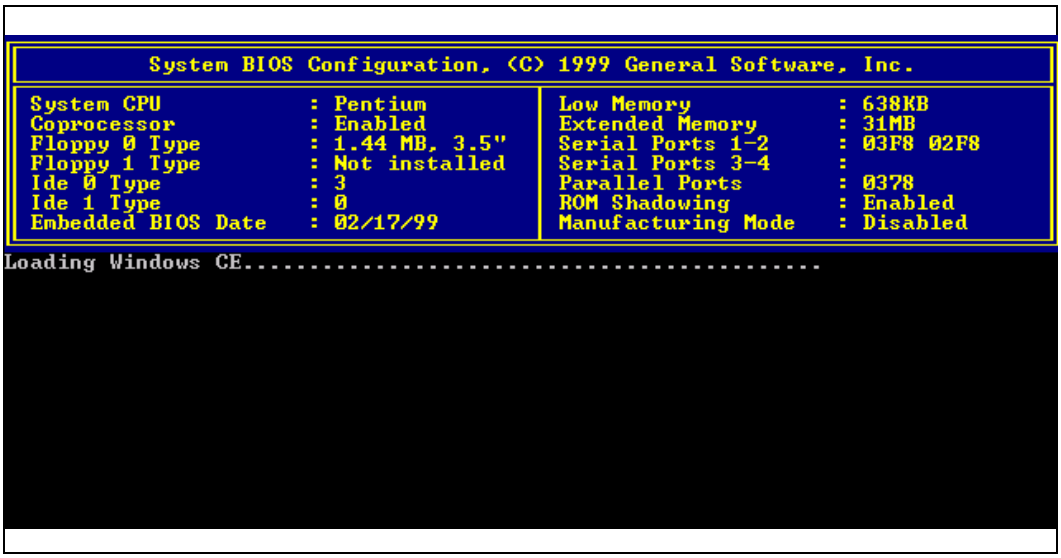
Caution: Hyperterminal's default setting is to use flow control, which will render the console inoperative. To change this, create a new session, change the flow control setting to "none," save the session, and exit Hyperterminal. Then reinvoke Hyperterminal with the session and it will operate with the new flow control setting.

5.5 CE-Ready—Windows CE Loader

Your TARGET's BIOS is CE-Ready and can directly boot Windows CE without loading an intermediate operating system such as DOS and LOADCEPC. Instead, the NK.BIN file can be placed on a disk drive or drive emulator, and then the BIOS can be configured through the Basic CMOS Configuration Setup Screen to boot the NK.BIN file from the boot drives instead of the boot records on those drives.

To configure your system to boot Windows CE natively from a disk drive, set the Boot Method field to "Windows CE" in the Basic CMOS Configuration Setup Screen. Then, place a copy of NK.BIN suitable for execution by LOADCEPC in the root directory of your normal boot drive, such as drive C:. Then, reboot the system. The configuration box should be displayed (Figure 15) followed by the message "Loading Windows CE…" This indicates that the loading process is continuing. Once fully loaded, Windows CE takes over the system and runs using the standard PC keyboard, screen, and PS/2 mouse.

Figure 15. The CE-Ready Feature

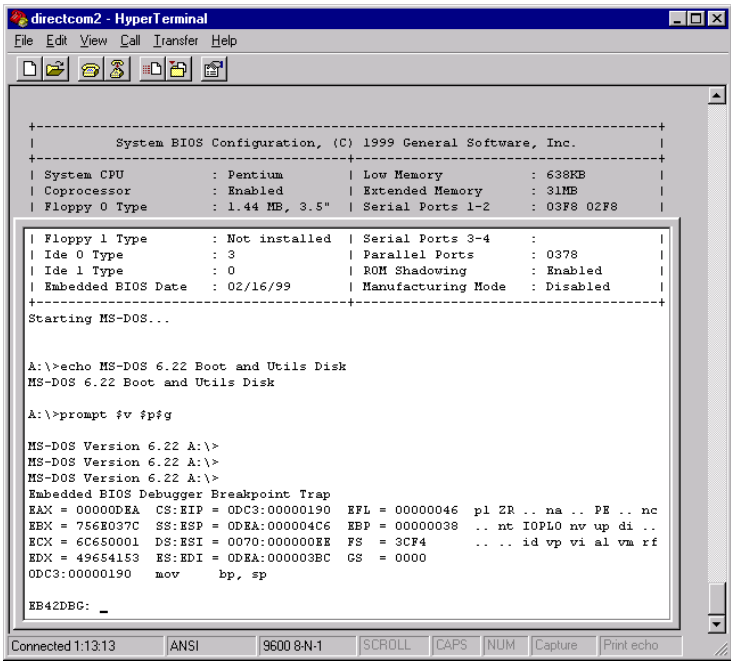


5.6 Integrated BIOS Debugger

The TARGET's BIOS contains a built-in debugger that can be a valuable tool to aid the board bring-up process on new designs similar to the reference board. It supports a DOS SYMDEB-style command line interface, and can be used on the main console's keyboard and screen, or over a redirected connection to a terminal program (see Section 5.4, above).

To activate the debugger at any time from the main console, press the left shift and the control keys together. A display similar to the one in the Hyperterminal session below (Figure 16) will appear, containing the title, "Embedded BIOS Debugger Breakpoint Trap" and a snapshot of the CPU general registers.

Figure 16. Integrated BIOS Debugger



To leave the debugger and resume the interrupted activity (whether POST, BIOS, DOS, Windows, or an application program), enter the “G” command (short for “go”) and press ENTER. If you were at a DOS prompt when you entered the debugger, then DOS will still be waiting for its command, and will not prompt again until you press ENTER again.

The debugger can also be entered from the Setup Screen System, and as a boot activity (see Basic CMOS Setup Screen), as a last ditch effort during board bring-up and development if no bootable device is available.

If your version of DOS, an application, or any OEM-supplied BIOS extensions have debugging code (i.e., “INT 3” instructions) remaining, then these will invoke the debugger automatically, although this is not an error. To continue, use the “G” command. When Embedded BIOS is adapted by the OEM, the debugger can be removed from the final production BIOS, and superfluous debugging code in the application will not cause the debugger to be invoked.

A complete discussion of the debugger is beyond the scope of this chapter; however, complete documentation is available from General Software.

5.7 Troubleshooting POST

This section provides a reference for debug aids useful in diagnosing booting.

5.7.1 Embedded BIOS POST Codes

To provide information to OEM developers about system faults, Embedded BIOS writes progress codes, also known as POST codes, to I/O port 80h during POST. These POST codes may be monitored by a port 80h card in either an ISA slot or PCI slot; they are not displayed on the screen. For more information about POST codes, contact General Software. Please note that the Embedded BIOS adaptation may be configured to reroute these codes over another I/O port or device.

Mnemonic Code	Code	System Progress Report
POST_STATUS_START	00h	Start POST (BIOS is executing)
POST_STATUS_CPUTEST	01h	Start CPU register test
POST_STATUS_DELAY	02h	Start power-on delay
POST_STATUS_DELAYDONE	03h	Power-on delay finished
POST_STATUS_KBDBATRDY	04h	Keyboard BAT finished
POST_STATUS_DISABSHADOW	05h	Disable shadowing & cache
POST_STATUS_CALCCKSUM	06h	Compute ROM CRC, wait for KBC
POST_STATUS_CKSUMGOOD	07h	CRC okay, KBC ready
POST_STATUS_BATVRFY	08h	Verifying BAT command to KB
POST_STATUS_KBDCMD	09h	Start KBC command
POST_STATUS_KBDDATA	0ah	Start KBC data
POST_STATUS_BLKUNBLK	0bh	Start pin 23,24 blocking & unblocking
POST_STATUS_KBDNOP	0ch	Start KBC NOP command
POST_STATUS_SHUTTEST	0dh	Test CMOS RAM shutdown register
POST_STATUS_CMOSDIAG	0eh	Check CMOS checksum
POST_STATUS_CMOSINIT	0fh	Initialize CMOS contents
POST_STATUS_CMOSSTATUS	10h	Initialize CMOS status for date/time
POST_STATUS_DISABDMAINT	11h	Disable DMA, PICs
POST_STATUS_DISABPORTB	12h	Disable Port B, video display
POST_STATUS_BOARD	13h	Initialize board, start memory detection
POST_STATUS_TESTTIMER	14h	Start timer tests
POST_STATUS_TESTTIMER2	15h	Test 8254 T2, for speaker, port B
POST_STATUS_TESTTIMER1	16h	Test 8254 T1, for refresh
POST_STATUS_TESTTIMER0	17h	Test 8254 T0, for 18.2Hz
POST_STATUS_MEMREFRESH	18h	Start memory refresh
POST_STATUS_TESTREFRESH	19h	Test memory refresh
POST_STATUS_TEST15US	1ah	Test 15usec refresh ON/OFF time
POST_STATUS_TEST64KB	1bh	Test base 64 Kbytes memory
POST_STATUS_TESTDATA	1ch	Test data lines
POST_STATUS_TESTADDR	20h	Test address lines
POST_STATUS_TESTPARITY	21h	Test parity (toggling)
POST_STATUS_TESTMEMRDWR	22h	Test Base 64 Kbytes memory

Mnemonic Code	Code	System Progress Report
POST_STATUS_SYSINIT	23h	Prepare system for IVT initialization
POST_STATUS_INITVECTORS	24h	Initialize vector table
POST_STATUS_8042TURBO	25h	Read 8042 for turbo switch setting
POST_STATUS_POSTTURBO	26h	Initialize turbo data
POST_STATUS_POSTVECTORS	27h	Modification of IVT
POST_STATUS_MONOMODE	28h	Video in monochrome mode verified
POST_STATUS_COLORMODE	29h	Video in color mode verified
POST_STATUS_TOGGLEPARITY	2ah	Toggle parity before video ROM test
POST_STATUS_INITBEFOREVIDEO	2bh	Initialize before video ROM check
POST_STATUS_VIDEOROM	2ch	Passing control to video ROM
POST_STATUS_POSTVIDEO	2dh	Control returned from video ROM
POST_STATUS_CHECKEGAVGA	2eh	Check for EGA/VGA adapter
POST_STATUS_TESTVIDEOMEMORY	2fh	No EGA/VGA found, test video memory
POST_STATUS_RETRACE	30h	Scan for video retrace signal
POST_STATUS_ALTDISPLAY	31h	Primary retrace failed
POST_STATUS_ALTRETRACE	32h	Alternate found
POST_STATUS_VRFYSWADAPTER	33h	Verify video switches
POST_STATUS_SETDISPMODE	34h	Establish display mode
POST_STATUS_CHECKSEG40A	35h	Initialize ROM BIOS data area
POST_STATUS_SETCURSOR	36h	Set cursor for power-on msg
POST_STATUS_PWRONDISPLAY	37h	Display power-on message
POST_STATUS_SAVECURSOR	38h	Save cursor position
POST_STATUS_BIOSIDENT	39h	Display BIOS identification string
POST_STATUS_HITDEL	3ah	Display “Hit <DEL> to ...” message
POST_STATUS_VIRTUAL	40h	Prepare protected mode test
POST_STATUS_DESCR	41h	Prepare descriptor tables
POST_STATUS_ENTERVM	42h	Enter virtual mode for memory test
POST_STATUS_ENABINT	43h	Enable interrupts for diagnostics mode
POST_STATUS_CHECKWRAP1	44h	Initialize data for memory wrap test
POST_STATUS_CHECKWRAP2	45h	Test for wrap, find total memory size
POST_STATUS_HIGHPATTERNS	46h	Write extended memory test patterns
POST_STATUS_LOWPATTERNS	47h	Write conventional memory test patterns
POST_STATUS_FINDLOWMEM	48h	Find low memory size from patterns
POST_STATUS_FINDHIMEM	49h	Find high memory size from patterns
POST_STATUS_CHECKSEG40B	4ah	Verify ROM BIOS data area again
POST_STATUS_CHECKDEL	4bh	Check for <DEL> pressed
POST_STATUS_CLREXTMEM	4ch	Clear extended memory for soft reset
POST_STATUS_SAVEMEMSIZE	4dh	Save memory size
POST_STATUS_COLD64TEST	4eh	Cold boot: Display 1st 64 Kbytes memtest

Mnemonic Code	Code	System Progress Report
POST_STATUS_COLDLOWTEST	4fh	Cold boot: Test all of low memory
POST_STATUS_ADJUSTLOW	50h	Adjust memory size for EBDA usage
POST_STATUS_COLDHITEST	51h	Cold boot: Test high memory
POST_STATUS_REALMODETEST	52h	Prepare for shutdown to real mode
POST_STATUS_ENTERREAL	53h	Return to real mode
POST_STATUS_SHUTDOWN	54h	Shutdown successful
POST_STATUS_DISABA20	55h	Disable A20 line
POST_STATUS_CHECKSEG40C	56h	Check ROM BIOS data area again
POST_STATUS_CHECKSEG40D	57h	Check ROM BIOS data area again
POST_STATUS_CLRHITDEL	58h	Clear “Hit <DEL>“ message
POST_STATUS_TESTDMAPAGE	59h	Test DMA page register file
POST_STATUS_VRFYDISPMEM	60h	Verify from display memory
POST_STATUS_TESTDMA0BASE	61h	Test DMA0 base register
POST_STATUS_TESTDMA1BASE	62h	Test DMA1 base register
POST_STATUS_CHECKSEG40E	63h	Checking ROM BIOS data area again
POST_STATUS_CHECKSEG40F	64h	Checking ROM BIOS data area again
POST_STATUS_PROGDMA	65h	Program DMA controllers
POST_STATUS_INITINTCTRL	66h	Initialize PICs
POST_STATUS_STARTKBDTEST	67h	Start keyboard test
POST_STATUS_KBDRESET	80h	Issue KB reset command
POST_STATUS_CHECKSTUCKKEYS	81h	Check for stuck keys
POST_STATUS_INITCIRCBUFFER	82h	Initialize circular buffer
POST_STATUS_CHECKLOCKEDKEYS	83h	Check for locked keys
POST_STATUS_MEMSIZEMISMATCH	84h	Check for memory size mismatch
POST_STATUS_PASSWORD	85h	Check for password or bypass setup
POST_STATUS_BEFORESETUP	86h	Password accepted
POST_STATUS_CALLSETUP	87h	Entering setup system
POST_STATUS_POSTSETUP	88h	Setup system exited
POST_STATUS_DISPPWRON	89h	Display power-on screen message
POST_STATUS_DISPWAIT	8ah	Display “Wait...” message
POST_STATUS_ENABSHADOW	8bh	Shadow system & video BIOS
POST_STATUS_STDCMOSSETUP	8ch	Load standard setup values from CMOS
POST_STATUS_MOUSE	8dh	Test and initialize mouse
POST_STATUS_FLOPPY	8eh	Test floppy disks
POST_STATUS_CONFIGFLOPPY	8fh	Configure floppy drives
POST_STATUS_IDE	90h	Test hard disks
POST_STATUS_CONFIGIDE	91h	Configure IDE drives
POST_STATUS_CHECKSEG40G	92h	Checking ROM BIOS data area
POST_STATUS_CHECKSEG40H	93h	Checking ROM BIOS data area

Mnemonic Code	Code	System Progress Report
POST_STATUS_SETMEMSIZE	94h	Set base & extended memory sizes
POST_STATUS_SIZEADJUST	95h	Adjust low memory size for EBDA
POST_STATUS_INITC8000	96h	Initialize before calling C800h ROM
POST_STATUS_CALLC8000	97h	Call ROM BIOS extension at C800h
POST_STATUS_POSTC8000	98h	ROM C800h extension returned
POST_STATUS_TIMERPRNBASE	99h	Configure timer/printer data
POST_STATUS_SERIALBASE	9ah	Configure serial port base addresses
POST_STATUS_INITBEFORENPX	9bh	Prepare to initialize coprocessor
POST_STATUS_INITNPX	9ch	Initialize numeric coprocessor
POST_STATUS_POSTNPX	9dh	Numeric coprocessor initialized
POST_STATUS_CHECKLOCKS	9eh	Check KB settings
POST_STATUS_ISSUEKBDID	9fh	Issue keyboard ID command
POST_STATUS_RESETID	0a0h	KB ID flag reset
POST_STATUS_TESTCACHE	0a1h	Test cache memory
POST_STATUS_DISPSOFTERR	0a2h	Display soft errors
POST_STATUS_TYPEMATIC	0a3h	Set keyboard typematic rate
POST_STATUS_MEMWAIT	0a4h	Program memory wait states
POST_STATUS_CLRSCR	0a5h	Clear screen
POST_STATUS_ENABPTYNMI	0a6h	Enable parity and NMIs
POST_STATUS_INITE000	0a7h	Initialize before calling ROM at E000h
POST_STATUS_CALLE000	0a8h	Call ROM BIOS extension at E000h
POST_STATUS_POSTE000	0a9h	ROM extension returned
POST_STATUS_DISPCONFIG	0b0h	Display system configuration box
POST_STATUS_INT19BOOT	00h	Call INT 19h bootstrap loader
POST_STATUS_LOWMEMEXH	0b1h	Test low memory exhaustively
POST_STATUS_EXTMEMEXH	0b2h	Test extended memory exhaustively
POST_STATUS_PCIENUM	0b3h	Enumerate PCI busses

5.8 Critical Error Beep Codes

Embedded BIOS tests much of the hardware early in POST before messages can be displayed on the screen. When system failures are encountered at these early stages, POST uses beep codes (a sequence of tones on the speaker) to identify the source of the error.

The following is a comprehensive list of POST beep codes for the system BIOS. BIOS extensions, such as VGA ROMs and SCSI adapter ROMs, may use their own beep codes, including short/long sequences, or possibly beep codes that sound like the ones below. When diagnosing a system failure, remove these adapters if possible before making a final determination of the actual POST test that failed.

Mnemonic Code	Beep Count	Description of Problem
POST_BEEP_REFRESH	1	Memory refresh is not working
POST_BEEP_PARITY	2	Parity error found in 1st 64KB of memory
POST_BEEP_BASE64KB	3	Memory test of 1st 64KB failed
POST_BEEP_TIMER	4	T1 timer test failed
POST_BEEP_CPU	5	CPU test failed
POST_BEEP_GATEA20	6	Gate A20 test failed
POST_BEEP_DMA	7	DMA page/base register test failed
POST_BEEP_VIDEO	8	Video controller test failed
POST_BEEP_KEYBOARD	9	Keyboard test failed
POST_BEEP_SHUTDOWN	10	CMOS shutdown register test failed
POST_BEEP_CACHE	11	External cache test failed
POST_BEEP_BOARD	12	General board initialization failed
POST_BEEP_LOWMEM	13	Exhaustive low memory test failed
POST_BEEP_EXTMEM	14	Exhaustive extended memory test failed
POST_BEEP_CMOS	15	CMOS restart byte test failed
POST_BEEP_ADDRESS_LINE	16	Address line test failed
POST_BEEP_DATA_LINE	17	Data line test failed
POST_BEEP_INTERRUPT	18	Interrupt controller test failed
POST_BEEP_PASSWORD	1	Incorrect password used to access SETUP

Bill of Materials A

Table 13. Bill of Materials (Sheet 1 of 7)

Reference Description	Description	Quantity	Manufacturer	Manufacturer Part Number
R45-46,R49,R108-110, R122,R302	Resistor, 100, 1%, 1/16W, 100PPM, 0603	8	DALE/VISHAY	CRCW0603-1000FRT1
R3,R9,R11-12,R20, R22-23,R7476,R7980, R85,R97-99,R105, R113,R124,R144, R166,R168,R186,R194, R198,R204,R259-260, R263-266,R294,R298, R303,R504	Resistor, 1K, 1%, 1/16W, 100PPM, 0603	36	DALE/VISHAY	CRCW0603-1001FRT1
R4,R6,R8,R13,R5761, R72,R77,R87,R8993, R116,R128,R137,R139, R158,R173,R184185, R188189,R192, R195-196,R200,202, R212,R215,R220, R232,R261-262, R268,R277,R284,R292, R296,R299,R500503, R506,R514-517	Resistor, 10K, 1%, 1/16W, 100PPM, 0603	54	DALE/VISHAY	CRCW0603-1002FRT1
R95,R115,R127,R33	Resistor, 100K, 1%, 1/16W, 100PPM, 0603	4	DALE/VISHAY	CRCW0603-1003FRT1
R102,R117,R126,R129	Resistor, 1.21K, 1%, 1/16W, 100PPM, 0603	4	DALE/VISHAY	CRCW0603-1211FRT1
R187,R191,R308-309	Resistor, 150, 1%, 1/16W, 100PPM, 0603	4	DALE/VISHAY	CRCW0603-1500FRT1
R106,R111,R118-120, R125,R134-136,R146, R148,R199	Resistor, 1.5K, 1%, 1/16W, 100PPM, 0603	12	DALE/VISHAY	CRCW0603-1501FRT1
R156-157,R162,R164	Resistor, 15K, 1%, 1/16W, 100PPM, 0603	4	DALE/VISHAY	CRCW0603-1502FRT1
R149,R167,R170	Resistor, 2K, 1%, 1/16W, 100PPM, 0603	3	DALE/VISHAY	CRCW0603-2001FRT2
R37,R50,R94,R505	Resistor, 221, 1%, 1/16W, 100PPM, 0603	4	DALE/VISHAY	CRCW0603-2210FRT1
R5,R7,R10,R301	Resistor, 2.21K, 1%, 1/16W, 100PPM, 0603	4	DALE/VISHAY	CRCW0603-2211FRT1
R15,R43,R81	Resistor, 22.1K, 1%, 1/16W, 100PPM, 0603	3	DALE/VISHAY	CRCW0603-2212FRT1
R16,R19,R21,R24,R44, R96,R509-510	Resistor, 232K, 1%, 1/16W, 100PPM, 0603	8	DALE/VISHAY	CRCW0603-2323FRT1
R175-176,R213	Resistor, 243, 1%, 1/16W, 100PPM, 0603	3	DALE/VISHAY	CRCW0603-2430FRT1

Table 13. Bill of Materials (Sheet 2 of 7)

Reference Description	Description	Quantity	Manufacturer	Manufacturer Part Number
R25-26,R47-48,R51-52, R55-56,R82-84,R107, R114,R130,R145, R178-183	Resistor, 2.74K, 1%, 1/16W, 100PPM, 0603	21	DALE/VISHAY	CRCW0603-2741FRT1
R53,R104,R305,R310, R312-313,R315322, R324,R325,R327-329	Resistor, 332, 1%, 1/16W, 100PPM, 0603	19	DALE/VISHAY	CRCW0603-3320FRT1
R112	Resistor, 3.92K, 1%, 1/16W, 100PPM, 0603	1	DALE/VISHAY	CRCW0603-3921FRT2
R18,R3334,R3841,R86, R171,R174,R197, R207-211,R214, R216-219,R248,R267	Resistor, 4.75K, 1%, 1/16W, 100PPM, 0603	23	DALE/VISHAY	CRCW0603-4751FRT1
R31	Resistor, 47.5K, 1%, 1/16W, 100PPM, 0603	1	DALE/VISHAY	CRCW0603-4752FRT2
R36,R42	Resistor, 475K, 1%, 1/16W, 100PPM, 0603	2	DALE/VISHAY	CRCW0603-4753FRT1
R30,R314	Resistor, 549, 1%, 1/16W, 100PPM, 0603	2	DALE/VISHAY	CRCW0603-5490FRT1
R238,R293	Resistor, 5.62K, 1%, 1/16W, 100PPM, 0603	2	DALE/VISHAY	CRCW0603-5621FRT1
R35,R54	Resistor, 562K, 1%, 1/16W, 100PPM, 0603	2	DALE/VISHAY	CRCW0603-5623FRT1
R28,R103	Resistor, 619, 1%, 1/16W, 100PPM, 0603	2	DALE/VISHAY	CRCW0603-6190FRT1
R29	Resistor, 66.5K, 1%, 1/16W, 100PPM, 0603	1	DALE/VISHAY	CRCW0603-6652FRT1
R32,R88,R131133, R138,R141-143, R153,R161,R511-512	Resistor, 8.25K, 1%, 1/16W, 100PPM, 0603	13	DALE/VISHAY	CRCW0603-8251FRT1
R121,R123	Resistor, 10, 1%, 1/16W, 200PPM, 0603	2	DALE/VISHAY	CRCW0603-10R0FRT1
R203,R269,R279-282, R285-291	Resistor, 22.1, 1%, 1/16W, 200PPM, 0603	13	DALE/VISHAY	CRCW0603-22R1FRT1
R159-160,R163,R165	Resistor, 27.4, 1%, 1/16W, 200PPM, 0603	4	DALE/VISHAY	CRCW0603-27R4FRT1
R140,R154,R222-230, R234-237,R239-242, R249-257,R297	Resistor, 33.2, 1%, 1/16W, 200PPM, 0603	29	DALE/VISHAY	CRCW0603-33R2FRT1
R190,R193	Resistor, 47.5, 1%, 1/16W, 200PPM, 0603	2	DALE/VISHAY	CRCW0603-47R5FRT1
R101,R172,R205	Resistor, 56.2, 1%, 1/16W, 200PPM, 0603	3	DALE/VISHAY	CRCW0603-56R2FRT2
R17,R67-71,R206, R270-276,R278,R513	Resistor, ZERO ohm, .05 ohm MAX, 0603	16	DALE/VISHAY	CRCW0603-000RT1

Table 13. Bill of Materials (Sheet 3 of 7)

Reference Description	Description	Quantity	Manufacturer	Manufacturer Part Number
R169	Resistor, 1M, 1%, 1/8W, 100PPM, 1206	1	DALE/VISHAY	CRCW1206-1004FRT2
R100	Resistor, 10, 1%, 1/8W, 100PPM, 1206	1	DALE/VISHAY	CRCW1206-10R0FRT1
R306-307	Resistor, 75, 1%, 1/8W, 100PPM, 1206	2	DALE/VISHAY	CRCW1206-75R0FRT1
R150-151,R507-508	Resistor, 2.7ohm, 5%, 1/8W, 400PPM, 1206	4	DALE/VISHAY	CRCW1206-2R7JRT2
R177	Resistor, .005, 1%, 2W, 20PPM, smt	1	IRC	OARS1R005FTR
R6266,R78,R147,R152, R155,R231,R233, R243-R247,R258,R283, R295,R300,R326	No loads	21		
C1,C5-8,C13-16, C35-37,C44-45,C51, C99,C112,C115,C157, C192,C204	Capacitor, mon cer, 1uF, +80-20, 25V, 1206	21	AVX	12063G105ZAT2A
C73,C300,C308,C311	Capacitor, mon cer, 10PF, 10%, 50V, 0603	4	AVX	06035A100KAT2A
C18-33,C38,C40-41, C53-55,C167	Capacitor, mon cer, 100P, 5%, 50V, 0603	23	AVX	06035A101JAT2A
C63-64,C107-108, C240-241	Capacitor, mon cer, 22P, 5%, 50V, 0603	6	AVX	06035A220JAT2A
C174-175,C219-220, C224,C231	Capacitor, mon cer, 47P, 5%, 50V, 0603	6	AVX	06035A470JAT2A
C34,C50,C57-60,C294, C297,C304	Capacitor, mon cer, 470P, 5%, 50V, 0603	9	AVX	06035A471JAT2A
C74,C86,C156,C163, C165,C299,C301-302, C305	Capacitor, mon cer, 1000P, 10%, 50V, 0603	9	AVX	06035C102KAT2A
C39,C52,C79,C83-85, C90-92,C101-103, C136-144,C177-178, C181-182,C226,C228-230,C244,C255-257, C261-262,C266, C317-323	Capacitor, mon cer, 0.01uF, 20%, 50V, 0603	43	AVX	06035C103K(M)AT2A

Table 13. Bill of Materials (Sheet 4 of 7)

Reference Description	Description	Quantity	Manufacturer	Manufacturer Part Number
C2,C4,C9,C11-12,C17, C46-49,C61-62,C65, C68-72,C75-78,C80, C87-89,C93-97,C100, C105-106,C113-114, C116-135,C145-146, C148-150,C152-154, C158-161,C166,C169-173,C176,C179-180, C183-185,	Capacitor, mon cer, 0.1uF, 20%, 16V, 0603	168	AVX	0603YC104K(M)AT2A
C188-191,C193-195, C197-199,C201-203, C205-215,C217218, C221,C225,C227, C232-239,C245-251, C259-260,C263-265, C268-271,C273-277, C279-289,C291-292, C295-296,C298, C306-307,C310, C313-316,C324-325, C501-505				
C164	Capacitor, mon cer, 1500p, 10%, 50V, 0603	1	AVX	06035C152KAT2A
C3,C10,C147	Capacitor, mon cer, 2200PF, 10%, 50V, 0603	3	AVX	06035C222KAT2A
C162,C168,C196,C200, C222-223,C254	Capacitor, alum, 1200uF, 20%, 25V, .197 radial	7	PANASONIC SANYO	EEUFC1E122 25MV1200AX or -GX
C56,C67	Capacitor, alum, 220uF, 20%, 25V, .197 radial	2	PANASONIC	EEUFC1E221B
C104,C111	Capacitor, alum, 150uF, 20%, 35V, .138 radial	2	PANASONIC	EEUFC1V151
C66,C109-110,C151, C155,C186-187,C216, C242-243,C252-253, C267,C272,C278,C290, C293,C309,C312	Capacitor, tant, 4.7UF, 20%, 10V, 3528	19	KEMET	T491B475K010AS
C81-82,C303,C500	Capacitor, tant, 22U, 20%, 16V, 7343	4	KEMET	T491D226K025AS-TR
C258	Capacitor, tant, 33U, 20%, 16V, 7343	1	KEMET	T491D336M016AS-TAPE
FB1-23	Inductor, ferrite bead, 3A, 30ohm@100MHz, 0805	23	MURATA ELECTR	BLM21P300SPT
L2	Inductor, 1.68uH, 13.9A, smt	1	PULSE	PE-53691T
L1	Inductor, 4.7uH, 10%, 30mA, DCR=1ohm, 0805	1	MURATA ELECTR	LQG21N4R7K10T1
D2-3	Diode, signal, 30V, 500mA, SOT23	2	GENERAL SEMICON PHILIPS	BAT54C BAT54C

Table 13. Bill of Materials (Sheet 5 of 7)

Reference Description	Description	Quantity	Manufacturer	Manufacturer Part Number
DS1	Diode, rectifier, 3A, 40V, smt	1	ON SEMI	MBRS340T3
D1	Diode, signal, 150mA, 75V, SOT23	1	VISHAY FAIRCHILD	MMBD4148-7 MMBD4148
Y3	Crystal, 32.768KHz tuning fork, thru-hole	1	FOX M-TRON	NC-38,32.768KHz MMCC-1
Y4	Crystal, 14.318 MHz, .005%, smt	1	FOX M-TRON	FPX-143-14.318MHz T/R SX2050P-14.31818MHz T/R
Y1	Crystal, 24.567MHz, 50PPM,	1	FOX	FE245F-20
Y2	Crystal, smt, 25.000MHz, .005%	1	EPSON	MA-406-25.000M-G
U9	IC, Digital temp monitor, SSOP16	1	TI	THMC10DBQR
U2-3	IC, Digital RS232 Driver, SO20	2	TI	SN75C185DWR
U7	IC, Digital LVC Hex Inverter, SO14	1	TI	SN74LVC06AD
U8	IC, Digital LVC Hex Inverter Schmitt-trigger, SO14	1	TI	SN74LVC14ADR
U50	IC, Digital HC Nand Gate, SO14	1	TI	SN74HC00ADR
U4	IC, Audio amplifier, stereo, 2W/ch, SOL14	1	NATIONAL SEMI	LM1877M-9
VR1	IC, Voltage Regulator, 3.3V@250mA, SOT223	1	SEMTECH	EZ5Z3L-S3.3 TR
U6	IC, EEPROM, 64X16, I2C, SO8	1	ATMEL CATALYST	AT93C46-10SC-1.8 T&R CAT93C46BS-TE13
U13	IC, 440MX chipset, 100MHz, BGA492	1	INTEL	FW82443MX100
U5	IC, 10/100 Ethernet controller, PCI, BGA196	1	INTEL	GD82559
U14	IC, Super I/O, PC98/99, 5V, PQFP100	1	SMC	FDC37M812 QFP
U15	IC, System clock generator, SSOP56	1	ICS	ICS9250BF-19
U12	IC, Power FET drivers, TSSOP14	1	ANALOG DEVICES	ADP3410KRU
U10	IC, Switching power regulator, TSSOP28	1	ANALOG DEVICES	ADP3421JRU
Q8-9	Transistor, FET, 30V, 12.5A, 9mohm@10v, SO8	2	SILICONIX/ VISHAY	SI4420DY
Q3-4	Transistor, FET, 60V, 115mA, SOT23	2	ON SEMI	2N7002LT1
Q7	Transistor, npn, 200V, 320mA, SOT223	1	ZETEX	ZVNL120GTA
Q1-2,Q12	Transistor, npn, 40V, 200mA, SOT23	3	ON SEMI	MMBT3904LT1
Q6	Transistor, pnp, 60V, 600mA, SOT23	1	ON SEMI	MMBT2907ALT1
Q5	Transistor, pnp, 80V, 8A, DPAK	1	ON SEMI	MJD45H11T4
S1	Audio speaker, 5v, 2.7KHz, thru-hole	1	GOLDEN PACIFIC	GB-0905EP-1

Table 13. Bill of Materials (Sheet 6 of 7)

Reference Description	Description	Quantity	Manufacturer	Manufacturer Part Number
D6-7	LED, green, 7-seg display, 10pin	2	AGILENT	HDSP-7801
D4	LED, green, 1206-smt	1	STANLEY	BG1101W-TR
D8	LED, yellow, 1206-smt	1	STANLEY	AY1101W-TR
F3	Fuse, resettable, 1.5A, 15V, smt	1	RAYCHEM	SMD150-2
F1-2,F4	Fuse, resettable, 1.1A, 30V, smt	3	RAYCHEM	SMD100-2
J7	Connector, Stacked RJ45 and Dual USB, with 10/100Base-T magnetics, and status LEDs	1	KYCON AMPHENOL BEL FUSE	GSP-B-S2-GG-9100 RJMG-7326-71-01 0812-1X1T-03
U1	IC, Audio codec, 'AC97, LQFP48	1	SIGMATEL	STAC9721T
J18	Connector, CompactFlash Type-II socket, r/a	1	3M	N7E50-7516HG-40
J9-11	Connector, PCI Edge Socket, 5V/32-bit	3	AMP	145154-8
J12	Connector, ITP Debug Header, 30pin	1	AMP	104068-3
J8	Connector, CD-ROM Audio Header, 4pin	1	JST	B 4B-PH-K
J4	Connector, PS/2 Dual Stack, 6pin mini-din	1	KYCON	KMDG-6S/6S-S4N
P1	Connector, CPU Fan, 3P w/ friction lock	1	AMP MOLEX	640456-3 22-23-2031
J1-3	Connector, 3.5mm Stereo Jack, r/a	3	RDI	SJ510C
J19	Connector, 10x2 r/a header, 0.1" spacing	1	MOLEX	10-88-3201
J16	Connector, Floppy Header, 34pin, shrouded	1	AMP	103308-7
J17	Connector, IDE Header, 40pin, shrouded	1	AMP	103308-8
J5-6	Connector, Serial 9pin Sub-D Plug, r/a	2	AMP	788754-2
J13	Connector, ATX Power, 20pin, straight, shrouded	1	MOLEX	39-29-9202
E1-26	Machine-applied pin	26	AMP	87623-4
U16	Socket, TSOP40, smt, w/ cover	1	YAMAICHI	IC197-4004-2000
J14-15	Socket, DIMM, 168pin, 3.3v non-buffered	2	AMP	390074-6
U11	Socket, uPGA-2, ZIF, 495pin	1	FOXCONN	PZ49505-2141-02
BS1	Battery Socket, 2032-type coin, w/ eject tab	1	MEMORY PROT DEV	BA2032
U17-18	IC, PLD, PAL22V10, PLCC28 (needs programmed)	2	LATTICE	PALCE22V10H-15JC/4
XU16	IC, flash, 512kx8, 80ns, TSOP40 (needs prog'd)	1	MICRON	MT28F004B5VG-6T

Schematics B

Schematics are provided for the following items listed below. Schematics are available from the Intel Developer's Web site in PDF format.

- Block diagram
- Routing guidelines
- Processor Part 1 and 2
- ITP socket
- 440MX part 1 and 2
- DIMM sockets
- Super I/O, BIOS and post code display
- IDE, Compact Flash and floppy connectors
- Serial, keyboard, mouse, USB connectors
- Power and front panel connectors
- 82559 Ethernet
- AC'97 CODEC and sound I/O
- PCI 1 and 2
- PCI 3
- Voltage regulators
- Pullup/Pulldown resistors

INTEL(R) 440MX SCALABLE LOW POWER BOARD

TABLE OF CONTENTS

REVISION HISTORY

A 08-06-01 Initial Revision A Schematics

B 09-20-01 Changes to the following:
Changed TEST# pullup on MX to 3VSB
Super I/O: added circuitry to generate AEN during DMA cycles (needed on SMSC SIO)

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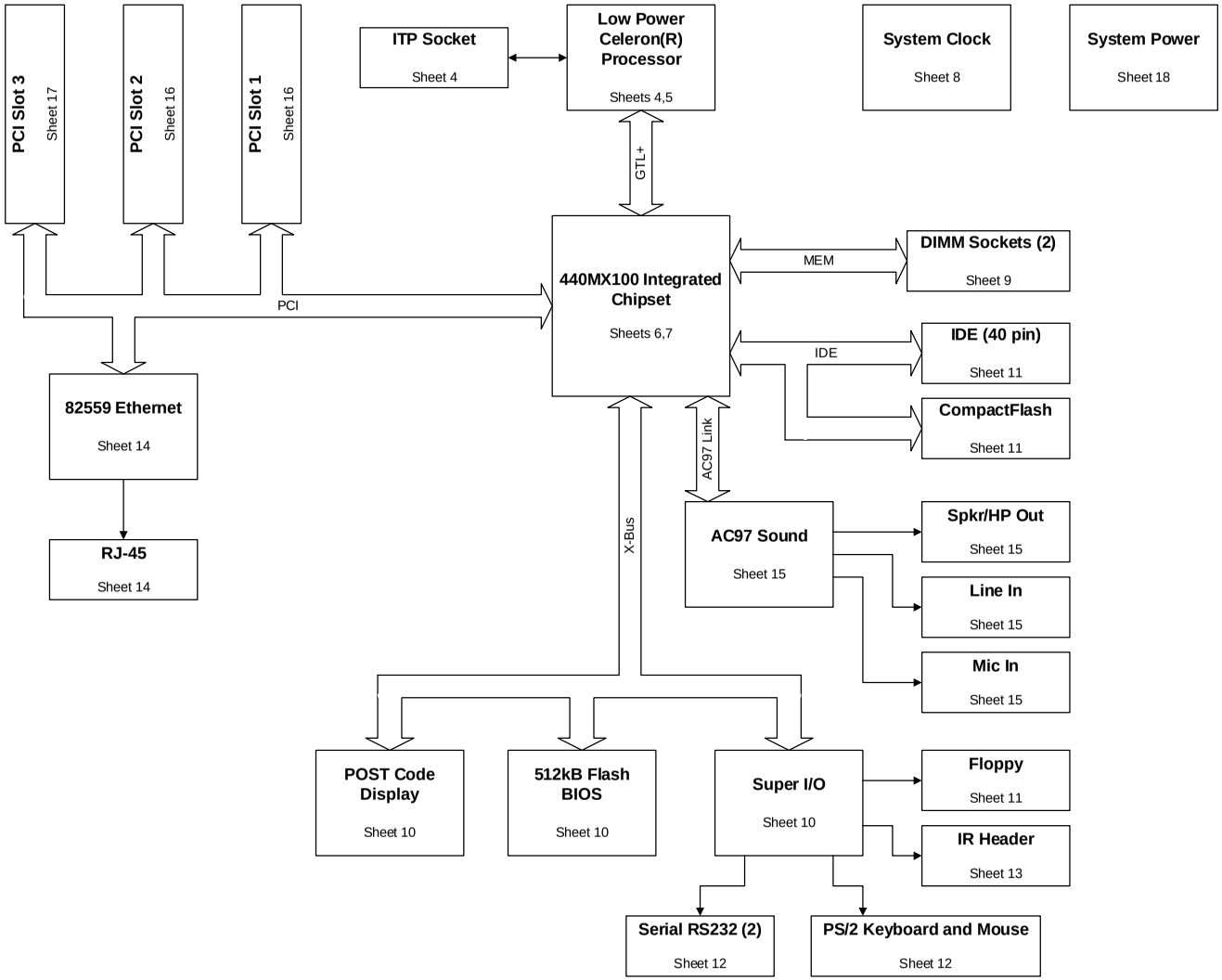
NOTE: ALL RESISTORS +/- 1%, ALL CAPACITORS +/- 20% UNLESS OTHERWISE NOTED

Intel Corporation
5000 W. Chandler Blvd.
Chandler, AZ 85226

TITLE: TABLE OF CONTENTS
REV: B
LAST: 09/20/01 10:29 AM
DATE: 05/30/01
B
DRAWING: 440MX SCALABLE LOW POWER BOARD
SHEET: 1 OF 19

INTEL(R) 440MX SCALABLE LOW POWER BOARD

BLOCK DIAGRAM



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Chandler, AZ 85226

TITLE: BLOCK DIAGRAM
REV: B
LAST: 09/20/01 10:29 AM
DATE: 05/30/01
B
DRAWING: 440MX SCALABLE LOW POWER BOARD
SHEET: 2 OF 19

INTEL(R) 440MX SCALABLE LOW POWER BOARD

ROUTING GUIDELINES

General Board Design Requirements

- Nominal trace impedance must be 65 ohms +/- 10%.
- Vias for decoupling capacitors must be kept as close as possible to capacitor pad.
- Finished board thickness is .062” +/- .007”.
- Outer layers must be ½ oz copper before plating, inner layers must be 1 oz copper.
- Series termination resistors must be kept as close to the driving pins as possible
- Signals with multiple endpoints should be daisy-chained, signal should not split into branches.
- GND plane must not be split
- Bypass capacitors on signals going to I/O connectors should be located as close to the connector as possible
- Check specific schematic pages for additional routing information

CPU Routing Requirements

- GTL+ signals between the CPU and 440MX should be between 1.9” and 4.3” long.
- Route GTL+ signals on layer adjacent to GND, and do not change layers.
- Signals between the CPU and 440MX must not differ in length by more than 1”.
- Spacing between adjacent signals should be as large as possible > 10 mils except for short distances for fanout. Total distance for fanout allowance is 250 mil.
- Route VREF_GTL signal as a minimum 25 mil trace, and keep 25 mil from other traces.
- Route CPU_PLL[2:1] using 25 mil trace, minimize loop area, and keep 25 mil from other traces.

Clock Specific Routing Requirements

- Series damping resistors must be less than 0.5” from clock IC.
- Clock traces should be routed on inner layers, with layer transitions at an absolute minimum.
- Spacing between clock trace and any other trace should be > 12 mils, serpentine spacing > 18 mils.
- MX_HCLK must be between 3.25” and 5.85” long, and CPU_HCLK must be 877 mils +/- 1 mil longer than MX_HCLK.
- ITP_HCLK should be the same length as CPU_HCLK.
- PCI clocks to the slots should be the same length, +/- 2”, but less than 12.5” long.
- Onboard PCI device clocks same as above, but 2.5” longer than PCI clocks to slots.
- MEM_CLKs to the DIMMs should be the same length, +/- 0.1”, and between 1.0” and 4” long.
- CLK_DCLKOUT should be the same length as the MEM_CLKs, +/- 0.1”.
- CLK_DCLKIN should be 2.5” longer than CLK_DCLKOUT, +/- 0.1”.

Switching Power Supply Routing Requirements

- Keep all unrelated signals and power planes away from switching regulator and related circuitry.
- Power input and output traces should be routed with minimal length while maximizing width.

Memory Bus Routing Requirements

- Length of MEM Bus lines should be between 1” and 4”.
- Spacing between other MEM Bus traces should be 10mil, spacing should be 5 mil for no more than 0.5”.
- Spacing to non-MEM Bus traces should be atleast 20 mil.
- MEM Bus traces should not transition between layers, except to get to the topside for the chipset.

PCI Bus Routing Requirements

- PCI signals should be similar length, routed in a daisy-chain fashion together to each component, with the 440MX as the last component.
- Total length of PCI signals must be less than 25”.

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NOTE: ALL RESISTORS +/- 1%, ALL CAPACITORS +/- 20% UNLESS OTHERWISE NOTED

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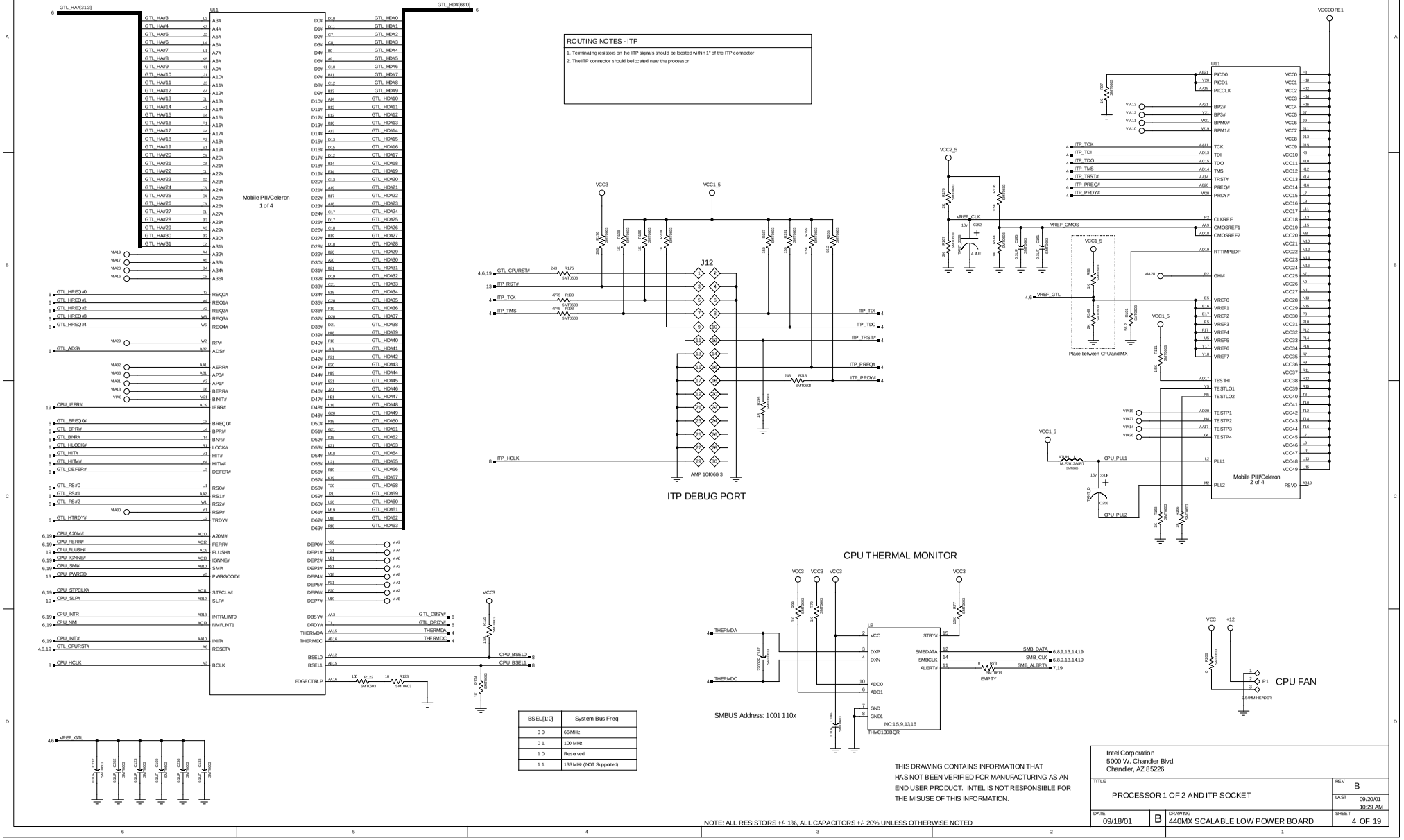
TITLE: ROUTING GUIDELINES
REV: B
LAST: 09/20/01 10:29 AM
DATE: 05/30/01
B
DRAWING: 440MX SCALABLE LOW POWER BOARD
SHEET: 3 OF 19


ROUTING NOTES - ITP
1. Terminating resistors on the ITP signals should be located within 1" of the ITP connector
2. The ITP connector should be located near the processor
Mobile PIII/Celeron
1 of 4
ITP DEBUG PORT
AMP 104068-3
CPU THERMAL MONITOR
SMBUS Address: 1001 110x
Mobile PIII/Celeron
2 of 4
Place between CPU and MX
CPU FAN
BSEL[1:0] | System Bus Freq
0 0 | 66 MHz
0 1 | 100 MHz
1 0 | Reserved
1 1 | 133 MHz (NOT Supported)
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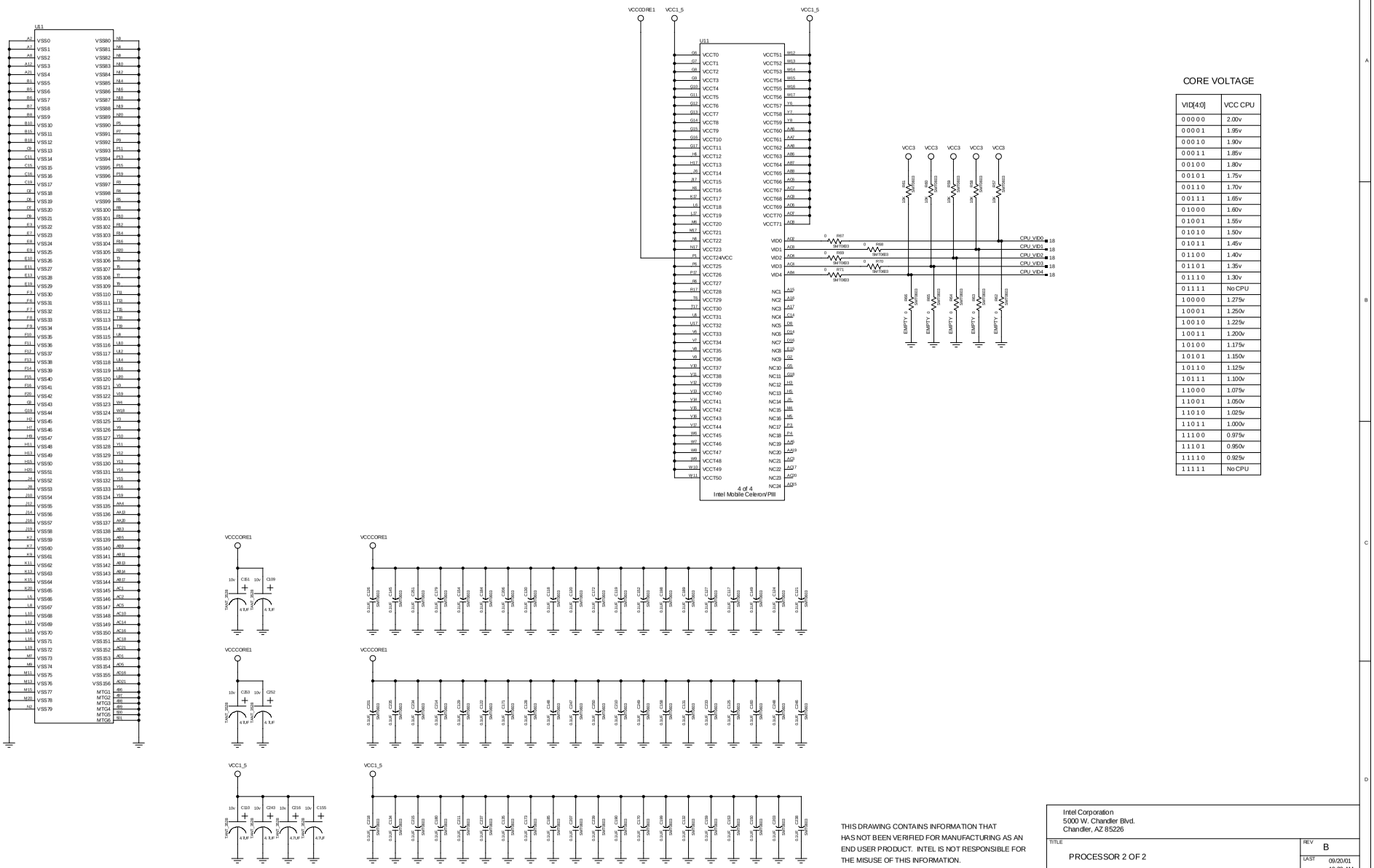
TITLE
PROCESSOR 1 OF 2 AND ITP SOCKET
REV B
LAST 09/20/01 10:29 AM
DATE 09/18/01
DRAWING 440MX SCALABLE LOW POWER BOARD
SHEET 4 OF 19



CORE VOLTAGE

VID[4:0]	VCC CPU
0 0 0 0 0	2.00v
0 0 0 0 1	1.95v
0 0 0 1 0	1.90v
0 0 0 1 1	1.85v
0 0 1 0 0	1.80v
0 0 1 0 1	1.75v
0 0 1 1 0	1.70v
0 0 1 1 1	1.65v
0 1 0 0 0	1.60v
0 1 0 0 1	1.55v
0 1 0 1 0	1.50v
0 1 0 1 1	1.45v
0 1 1 0 0	1.40v
0 1 1 0 1	1.35v
0 1 1 1 0	1.30v
0 1 1 1 1	No CPU
1 0 0 0 0	1.275v
1 0 0 0 1	1.250v
1 0 0 1 0	1.225v
1 0 0 1 1	1.200v
1 0 1 0 0	1.175v
1 0 1 0 1	1.150v
1 0 1 1 0	1.125v
1 0 1 1 1	1.100v
1 1 0 0 0	1.075v
1 1 0 0 1	1.050v
1 1 0 1 0	1.025v
1 1 0 1 1	1.000v
1 1 1 0 0	0.975v
1 1 1 0 1	0.950v
1 1 1 1 0	0.925v
1 1 1 1 1	No CPU

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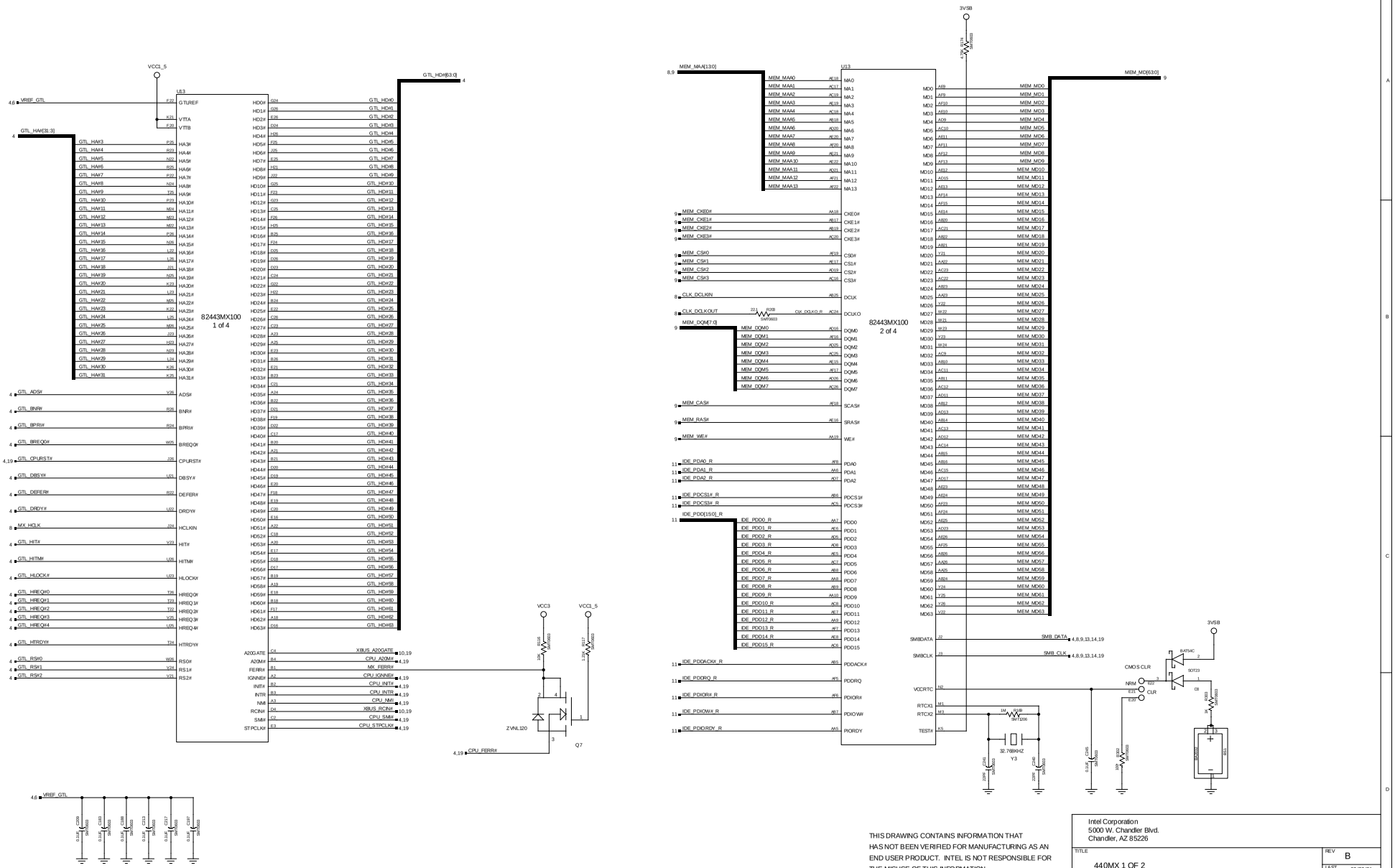
TITLE: PROCESSOR 2 OF 2		REV: B	
		LAST: 09/20/01 10:29 AM	
DATE: 09/18/01	B	DRAWING: 440MX SCALABLE LOW POWER BOARD	SHEET: 5 OF 19


82443MX100
1 of 4
82443MX100
2 of 4
U13
U13
VCC1_5
3VSB
GTL_HA#[31:3]
GTL_HD#[63:0]
MEM_MA#[13:0]
MEM_MD[63:0]
VREF_GTL
GTUREF
VTTA
VTTB
ADS#
BNR#
BPRI#
BREQ0#
CPURST#
DBSY#
DEFER#
DRDY#
HCLKIN
HIT#
HITM#
HLOCK#
HREQ0#
HREQ1#
HREQ2#
HREQ3#
HREQ4#
HTRDY#
RS0#
RS1#
RS2#
A20GATE
A20M#
FERR#
IGNNE#
INIT#
INTR
NMI
RCIN#
SMI#
STPCLK#
XBUS_A20GATE
CPU_A20M#
MX_FERR#
CPU_IGNNE#
CPU_INIT#
CPU_INTR
CPU_NMI
XBUS_RCIN#
CPU_SMI#
CPU_STPCLK#
CPU_FERR#
MEM_MA0
MEM_MA1
MEM_MA2
MEM_MA3
MEM_MA4
MEM_MA5
MEM_MA6
MEM_MA7
MEM_MA8
MEM_MA9
MEM_MA10
MEM_MA11
MEM_MA12
MEM_MA13
MEM_CKE0#
MEM_CKE1#
MEM_CKE2#
MEM_CKE3#
MEM_CS#0
MEM_CS#1
MEM_CS#2
MEM_CS#3
CLK_DCLKIN
CLK_DCLKOUT
CLK_DCLKO_R
MEM_DQM[7:0]
MEM_DQM0
MEM_DQM1
MEM_DQM2
MEM_DQM3
MEM_DQM4
MEM_DQM5
MEM_DQM6
MEM_DQM7
MEM_CAS#
MEM_RAS#
MEM_WE#
IDE_PDA0_R
IDE_PDA1_R
IDE_PDA2_R
IDE_PDCS1#_R
IDE_PDCS3#_R
IDE_PDD[15:0]_R
IDE_PDD0_R
IDE_PDD1_R
IDE_PDD2_R
IDE_PDD3_R
IDE_PDD4_R
IDE_PDD5_R
IDE_PDD6_R
IDE_PDD7_R
IDE_PDD8_R
IDE_PDD9_R
IDE_PDD10_R
IDE_PDD11_R
IDE_PDD12_R
IDE_PDD13_R
IDE_PDD14_R
IDE_PDD15_R
IDE_PDDACK#_R
IDE_PDDRQ_R
IDE_PDIOR#_R
IDE_PDIOW#_R
IDE_PDIORDY_R
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
MD8
MD9
MD10
MD11
MD12
MD13
MD14
MD15
MD16
MD17
MD18
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MD21
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MD23
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MD41
MD42
MD43
MD44
MD45
MD46
MD47
MD48
MD49
MD50
MD51
MD52
MD53
MD54
MD55
MD56
MD57
MD58
MD59
MD60
MD61
MD62
MD63
SMBDATA
SMBCLK
VCCRTC
RTCX1
RTCX2
TEST#
SMB_DATA
SMB_CLK
CMOS CLR
NRM
CLR
32.768KHZ
Y3
Z-VNL120
Q7
BAT54C
SOT23
D3
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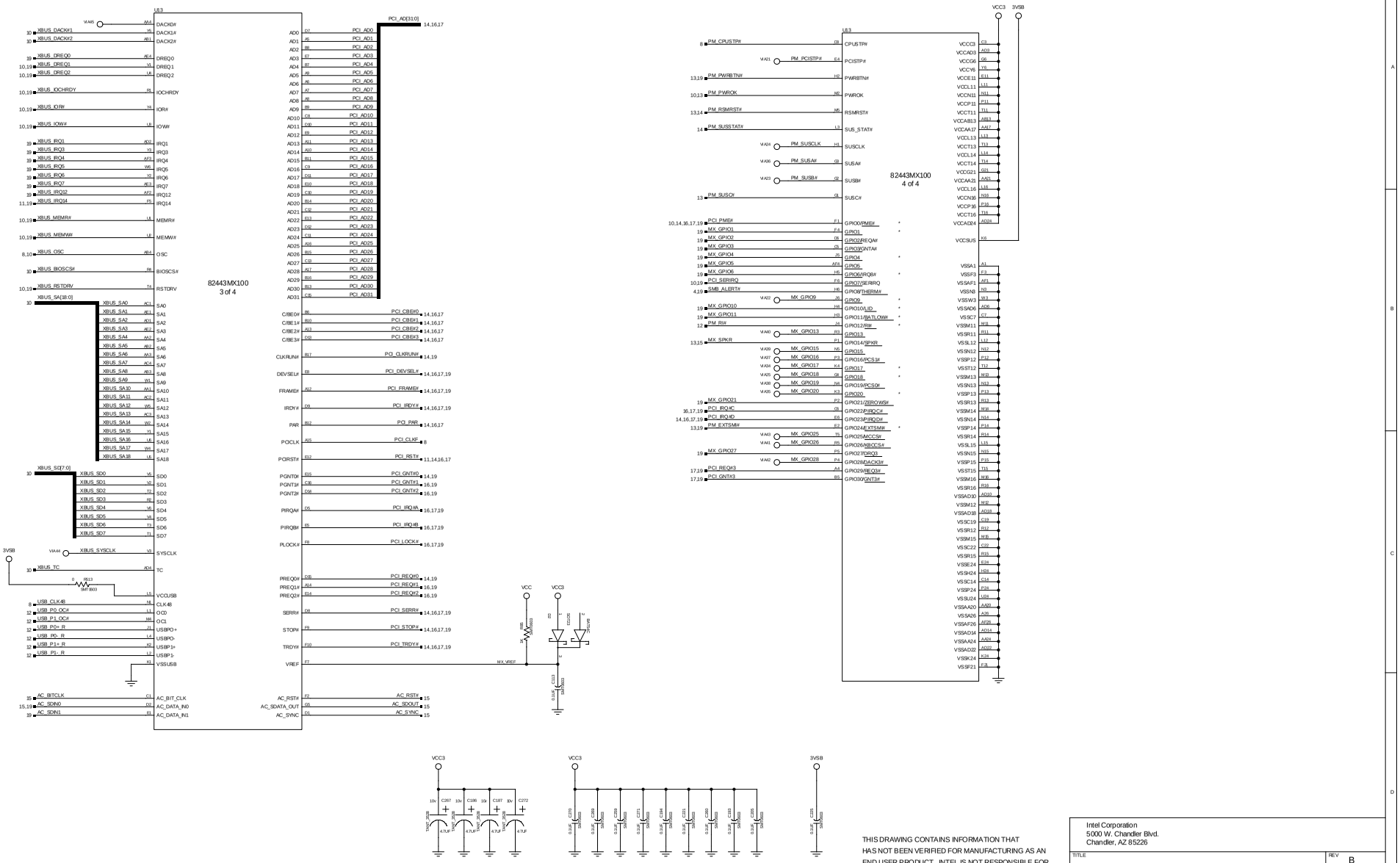
TITLE
440MX 1 OF 2
REV
B
LAST
09/20/01
10:29 AM
DATE
09/18/01
B
DRAWING
440MX SCALABLE LOW POWER BOARD
SHEET
6 OF 19



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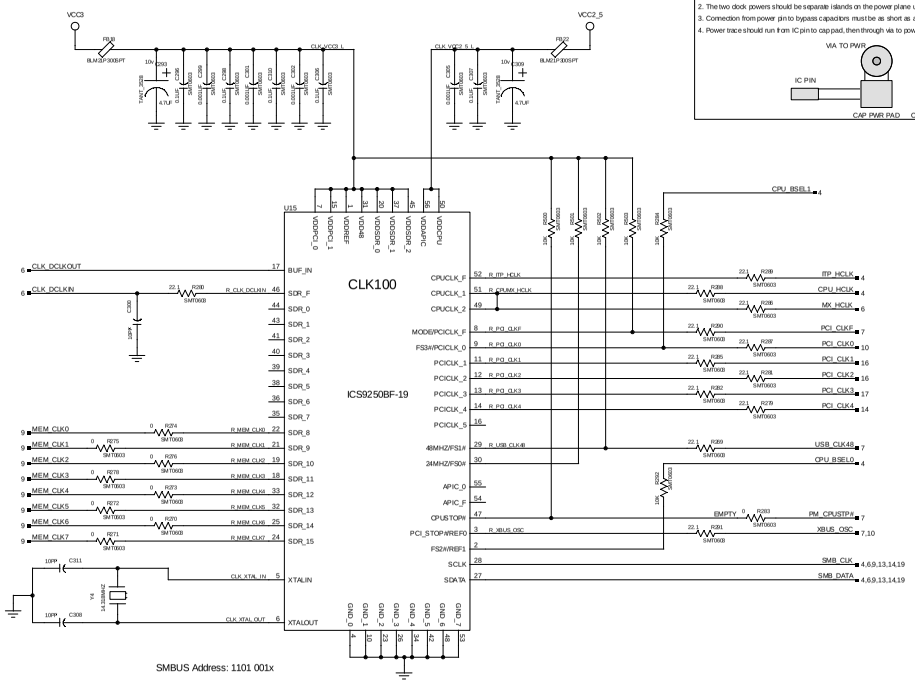
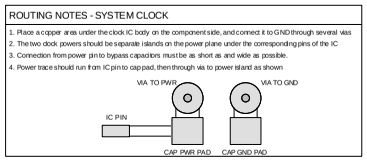
TITLE: 440MX 2 OF 2		REV: B	
		LAST: 09/20/01 10:29 AM	
DATE: 09/18/01	B	DRAWING: 440MX SCALABLE LOW POWER BOARD	SHEET: 7 OF 19

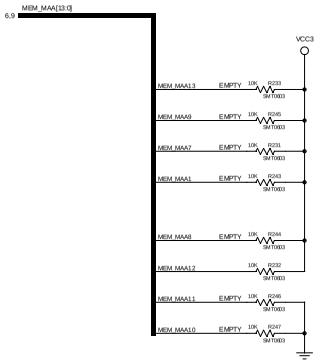




JUMPER DEFINITION TABLE

JUMPER	FUNCTION	JUMPER INSTALLATION OPTIONS	
CMOS CLR	Clear the RTC CMOS	CLR = Clear	NRM = Normal
BIOS UNLOCK	Install to Reprogram the BIOS	Installed = Unlocked	Not Installed = Locked
CF MASTER	Install to Set the CompactFlash as Master	Installed = CF Master	Not Installed = CF Slave
ENET ENA/DIS	Enable or Disable the Ethernet Controller	ENA = Enabled	DIS = Disabled

Indicates Default Jumper Location



STRAPPING OPTIONS

SIGNAL	FUNCTION	PULLDOWN	PULLUP	440MX DEFAULT
MA13	Processor Core/Bus Ratio Select (not used)	NMI Low	NMI High	PULLDOWN
MA9	Processor Core/Bus Ratio Select (not used)	INTR Low	INTR High	PULLDOWN
MA7	Processor Core/Bus Ratio Select (not used)	IGNNE# Low	IGNNE# High	PULLDOWN
MA1	Processor Core/Bus Ratio Select (not used)	A20M# Low	A20M# High	PULLDOWN
MA12	Host Frequency Select	66MHz	100MHz	PULLDOWN
MA11	In-Order Queue Depth Enable	One	Max	PULLUP
MA10	Quick Start Select	Disable	Enable	PULLUP
MA8	Reserved	Default	Reserved	PULLDOWN

Board Stuffing Default

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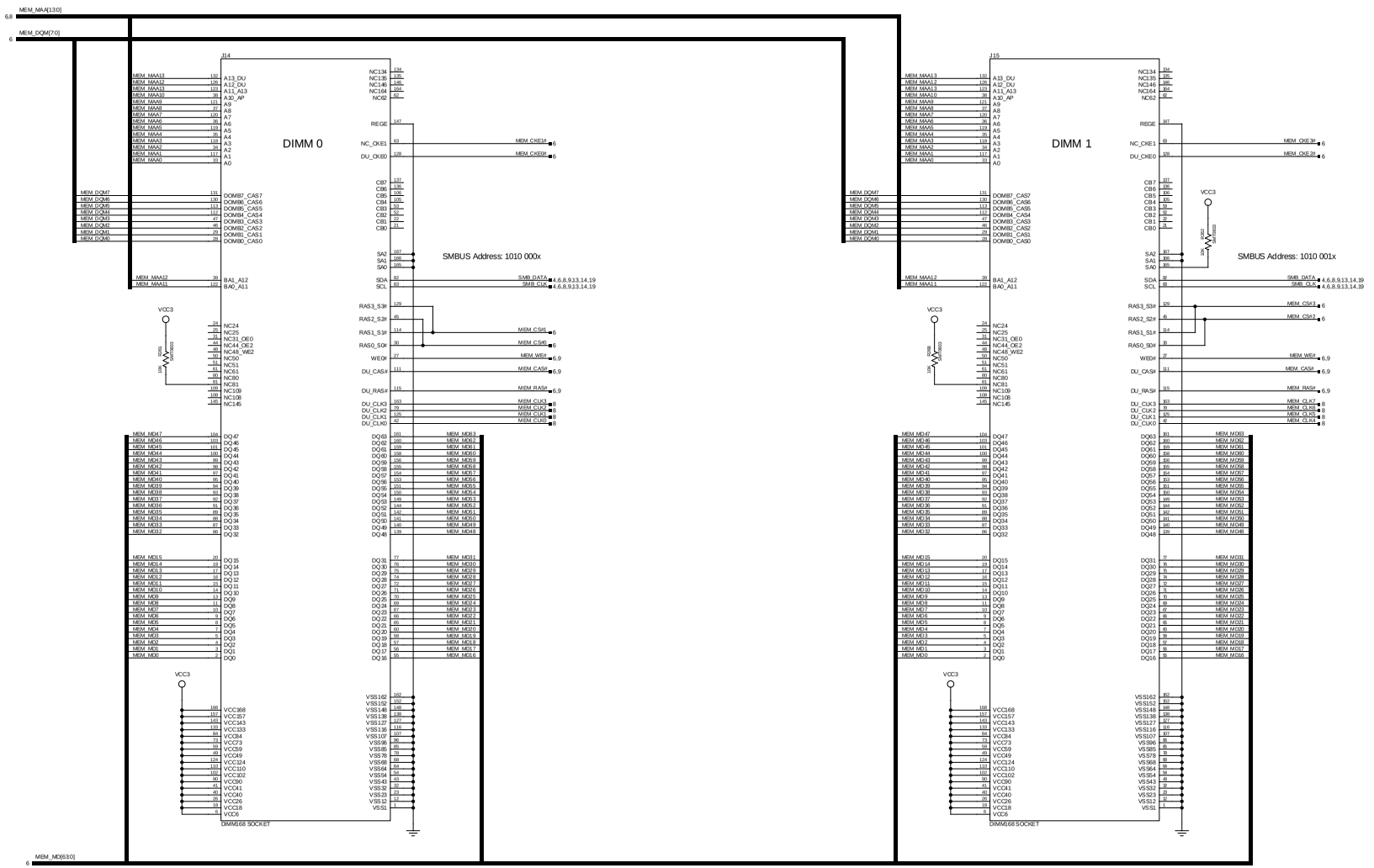
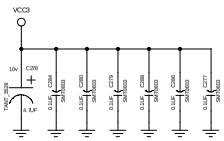
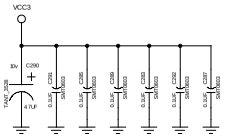
TITLE	SYSTEM CLOCK & STRAPPING OPTIONS	REV	B
		LAST	09/20/01 10:29 AM
DATE	09/18/01	DRAWING	440MX SCALABLE LOW POWER BOARD
	B	SHEET	8 OF 19







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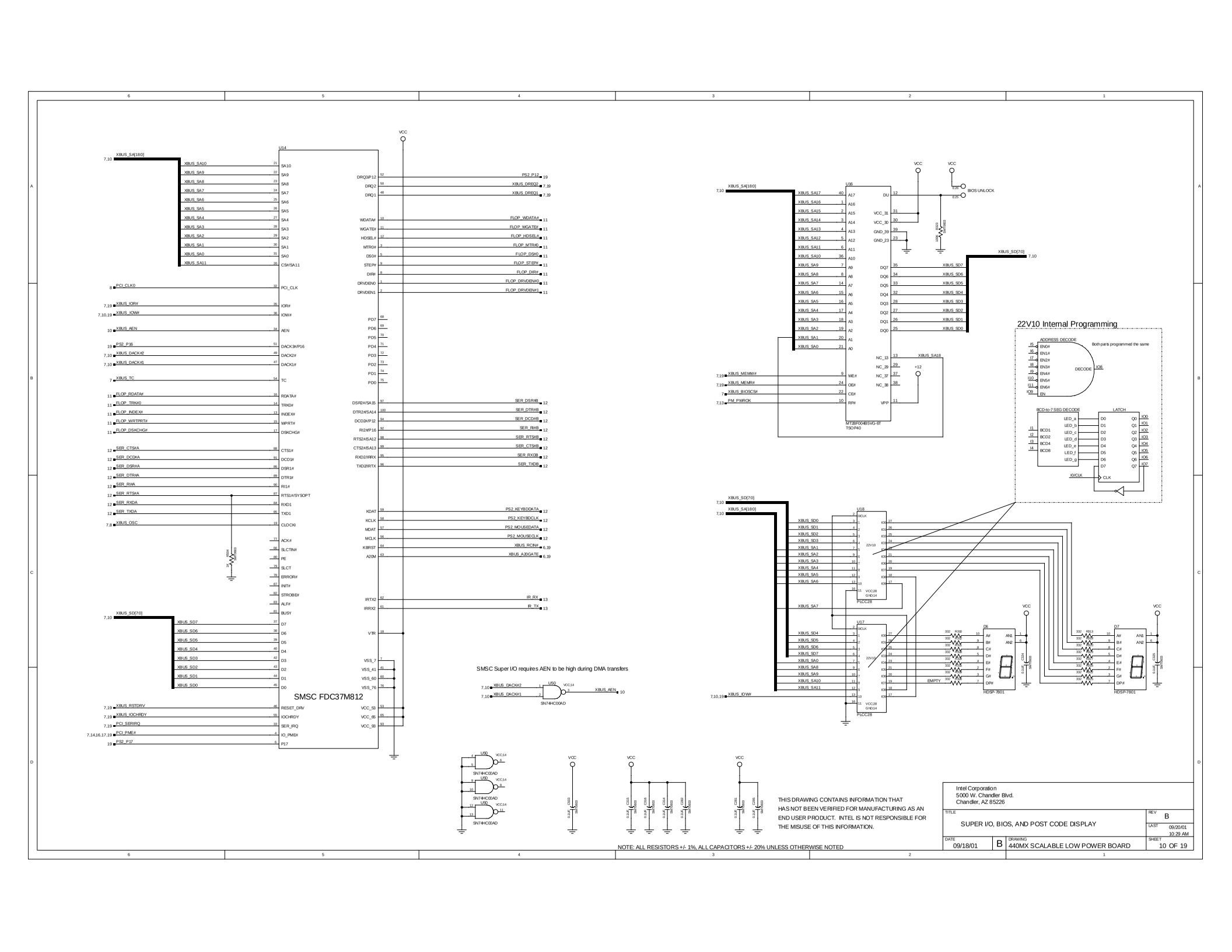
TITLE: DIMM SOCKETS		REV: B	
		LAST: 09/20/01 10:29 AM	
DATE: 09/18/01	B	DRAWING: 440MX SCALABLE LOW POWER BOARD	SHEET: 9 OF 19


SMSC FDC37M812
SMSC Super I/O requires AEN to be high during DMA transfers
22V10 Internal Programming
ADDRESS DECODE
Both parts programmed the same
DECODE
BCD-to-7 SEG DECODE
LATCH
BIOS UNLOCK
SN74HC00AD
PLCC28
HDSP-7801
MT28F004B5VG-6T
TSOP40
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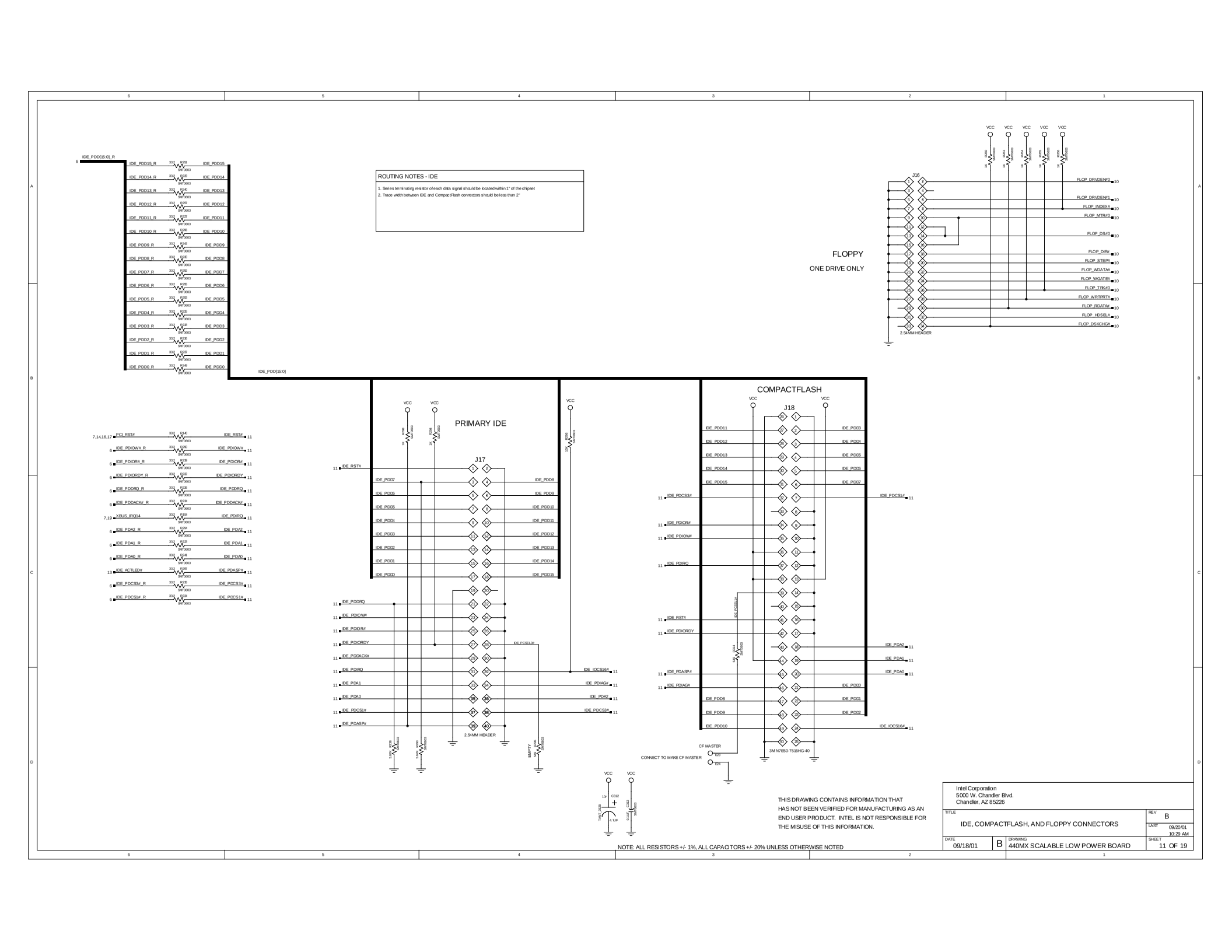
SUPER I/O, BIOS, AND POST CODE DISPLAY
REV B
LAST 09/20/01 10:29 AM
DATE 09/18/01
B
DRAWING 440MX SCALABLE LOW POWER BOARD
SHEET 10 OF 19


IDE_PDD[15:0]_R
IDE_PDD15_R
IDE_PDD14_R
IDE_PDD13_R
IDE_PDD12_R
IDE_PDD11_R
IDE_PDD10_R
IDE_PDD9_R
IDE_PDD8_R
IDE_PDD7_R
IDE_PDD6_R
IDE_PDD5_R
IDE_PDD4_R
IDE_PDD3_R
IDE_PDD2_R
IDE_PDD1_R
IDE_PDD0_R
IDE_PDD[15:0]
ROUTING NOTES - IDE
1. Series terminating resistor of each data signal should be located within 1" of the chipset
2. Trace width between IDE and CompactFlash connectors should be less than 2"
FLOPPY
ONE DRIVE ONLY
J16
FLOP_DRVDEN#0
FLOP_DRVDEN#1
FLOP_INDEX#
FLOP_MTR#0
FLOP_DS#0
FLOP_DIR#
FLOP_STEP#
FLOP_WDATA#
FLOP_WGATE#
FLOP_TRK#0
FLOP_WRTPRT#
FLOP_RDATA#
FLOP_HDSEL#
FLOP_DSKCHG#
2.54MM HEADER
PRIMARY IDE
J17
IDE_RST#
IDE_PDD7
IDE_PDD6
IDE_PDD5
IDE_PDD4
IDE_PDD3
IDE_PDD2
IDE_PDD1
IDE_PDD0
IDE_PDD8
IDE_PDD9
IDE_PDD10
IDE_PDD11
IDE_PDD12
IDE_PDD13
IDE_PDD14
IDE_PDD15
IDE_PDDRQ
IDE_PDIOW#
IDE_PDIOR#
IDE_PDIORDY
IDE_PDDACK#
IDE_PDIRQ
IDE_PDA1
IDE_PDA0
IDE_PDCS1#
IDE_PDASP#
IDE_PC3EL0#
IDE_IOCS16#
IDE_PDA0#
IDE_PDA2
IDE_PDCS3#
2.54MM HEADER
COMPACTFLASH
J18
IDE_PDD11
IDE_PDD12
IDE_PDD13
IDE_PDD14
IDE_PDD15
IDE_PDD3
IDE_PDD4
IDE_PDD5
IDE_PDD6
IDE_PDD7
IDE_PDCS3#
IDE_PDCS1#
IDE_PDIOR#
IDE_PDIOW#
IDE_PDIRQ
IDE_RST#
IDE_PDIORDY
IDE_PDA2
IDE_PDA1
IDE_PDA0
IDE_PDASP#
IDE_PDA0#
IDE_PDD0
IDE_PDD8
IDE_PDD1
IDE_PDD9
IDE_PDD2
IDE_PDD10
IDE_IOCS16#
CF MASTER
CONNECT TO MAKE CF MASTER
3M N7E50-7530HG-40
PC1_RST#
IDE_PDIOW#_R
IDE_PDIOR#_R
IDE_PDIORDY_R
IDE_PDDRQ_R
IDE_PDDACK#_R
XBUS_IRQ14
IDE_PDA2_R
IDE_PDA1_R
IDE_PDA0_R
IDE_ACTLED#
IDE_PDCS3#_R
IDE_PDCS1#_R
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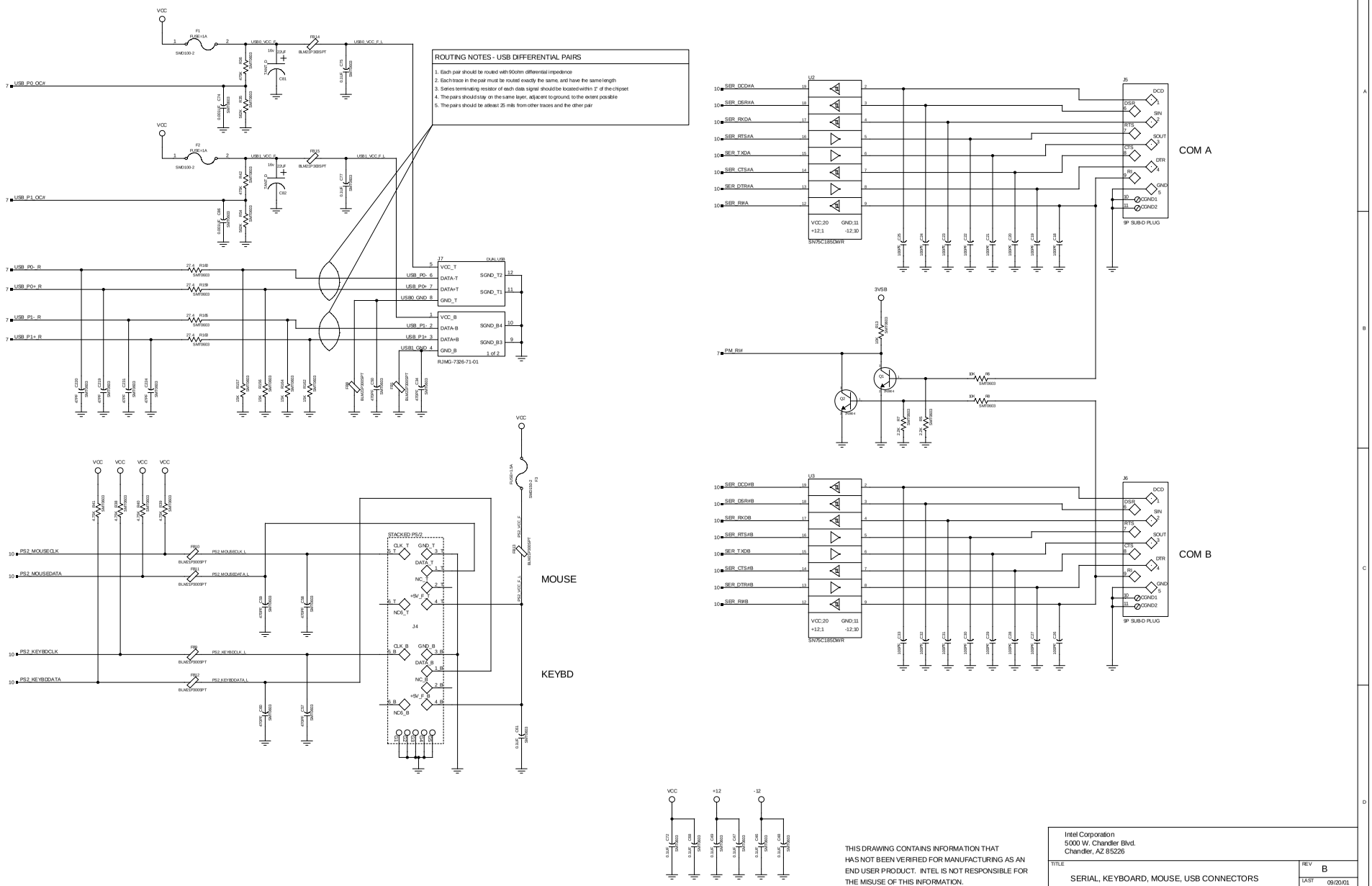
TITLE
IDE, COMPACTFLASH, AND FLOPPY CONNECTORS
REV B
LAST 09/20/01 10:29 AM
DATE 09/18/01
B
DRAWING 440MX SCALABLE LOW POWER BOARD
SHEET 11 OF 19



THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

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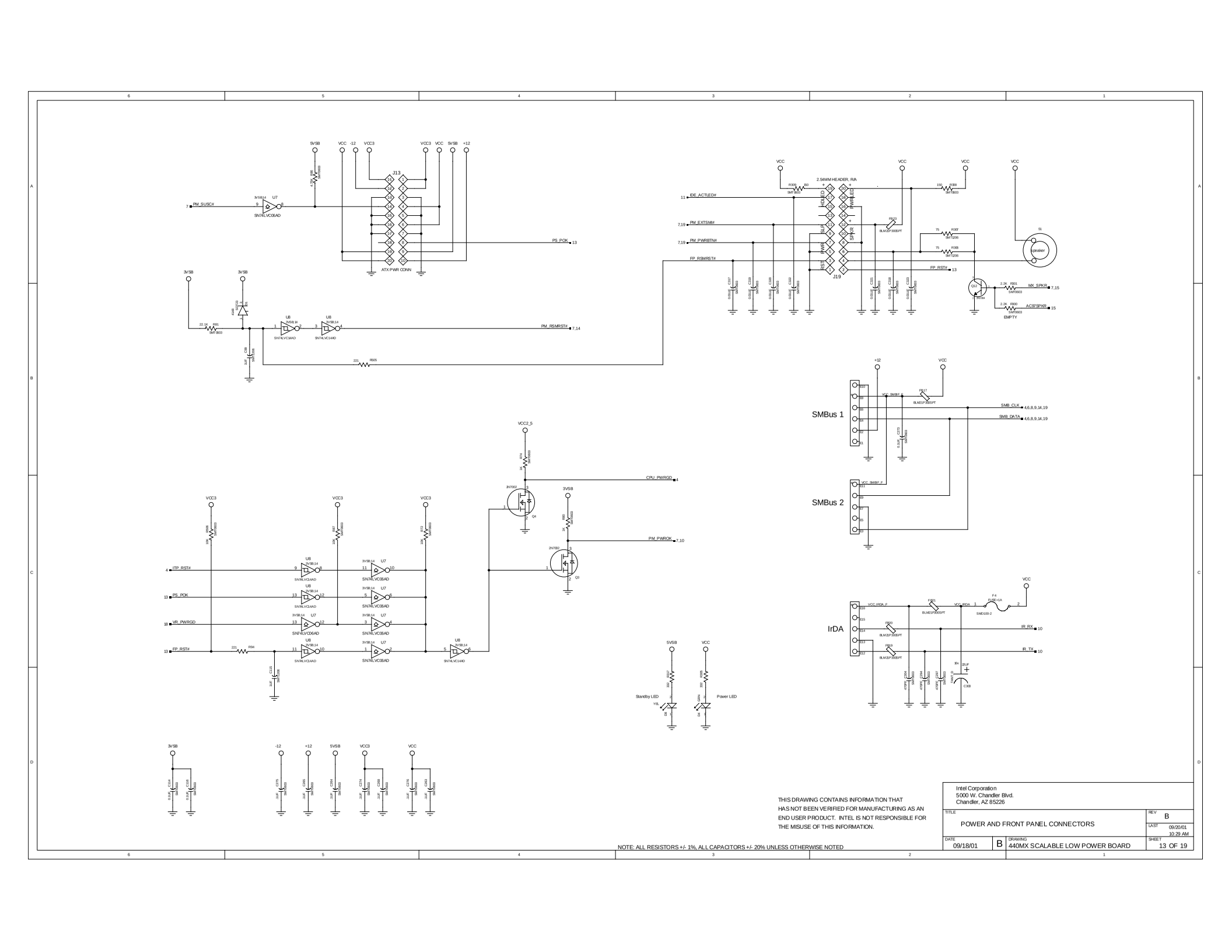
TITLE: SERIAL, KEYBOARD, MOUSE, USB CONNECTORS		REV: B	
		LAST: 09/20/01 10:29 AM	
DATE: 09/18/01	B	DRAWING: 440MX SCALABLE LOW POWER BOARD	SHEET: 12 OF 19



THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

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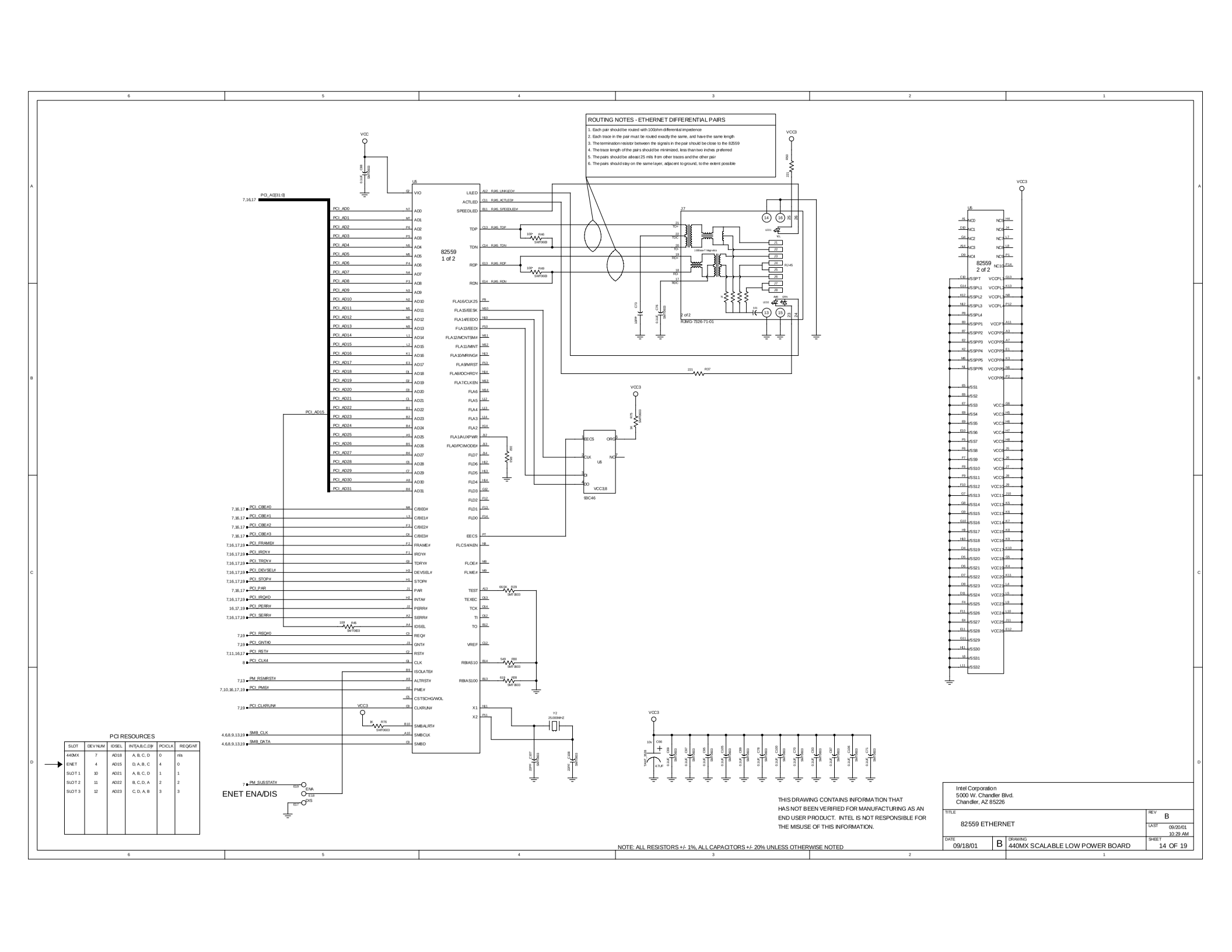
TITLE: POWER AND FRONT PANEL CONNECTORS		REV: B	
		LAST: 09/20/01 10:29 AM	
DATE: 09/18/01	B	DRAWING: 440MX SCALABLE LOW POWER BOARD	SHEET: 13 OF 19


ROUTING NOTES - ETHERNET DIFFERENTIAL PAIRS
1. Each pair should be routed with 100ohm differential impedence
2. Each trace in the pair must be routed exactly the same, and have the same length
3. The termination resistor between the signals in the pair should be close to the 82559
4. The trace length of the pairs should be minimized, less than two inches preferred
5. The pairs should be atleast 25 mils from other traces and the other pair
6. The pairs should stay on the same layer, adjacent to ground, to the extent possible
82559
1 of 2
82559
2 of 2
RJMG-7326-71-01
93C46
ENET ENA/DIS
PCI RESOURCES
SLOT | DEV NUM | IDSEL | INT[A,B,C,D]# | PCICLK | REQ/GNT
440MX | 7 | AD18 | A, B, C, D | 0 | n/a
ENET | 4 | AD15 | D, A, B, C | 4 | 0
SLOT 1 | 10 | AD21 | A, B, C, D | 1 | 1
SLOT 2 | 11 | AD22 | B, C, D, A | 2 | 2
SLOT 3 | 12 | AD23 | C, D, A, B | 3 | 3
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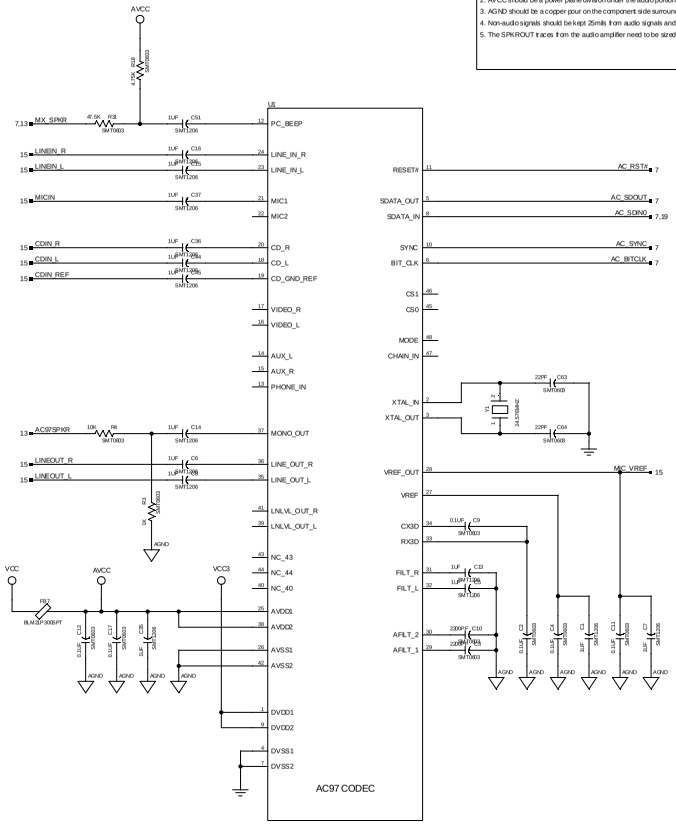
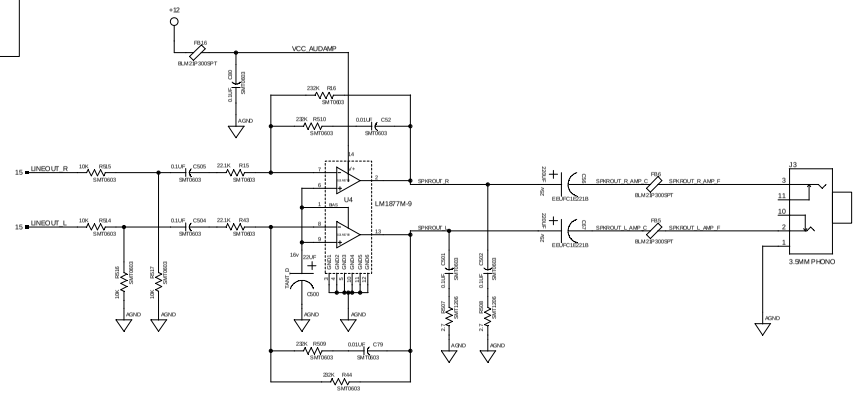
TITLE
82559 ETHERNET
REV B
LAST 09/20/01 10:29 AM
DATE 09/18/01
B
DRAWING 440MX SCALABLE LOW POWER BOARD
SHEET 14 OF 19

ROUTING NOTES - AUDIO SIGNALS

1. The audio portion of the codec includes all signals coming from pins 13 thru 44 of the codec
2. AVCC should be a power plane division under the audio portion of the IC and all audio traces and components
3. AGND should be a copper pour on the component side surrounding the audio traces and components
4. Non-audio signals should be kept 25mils from audio signals and also AGND
5. The SPKROUT traces from the audio amplifier need to be sized to handle 1A each





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TITLE: AC97 AUDIO		REV: B	
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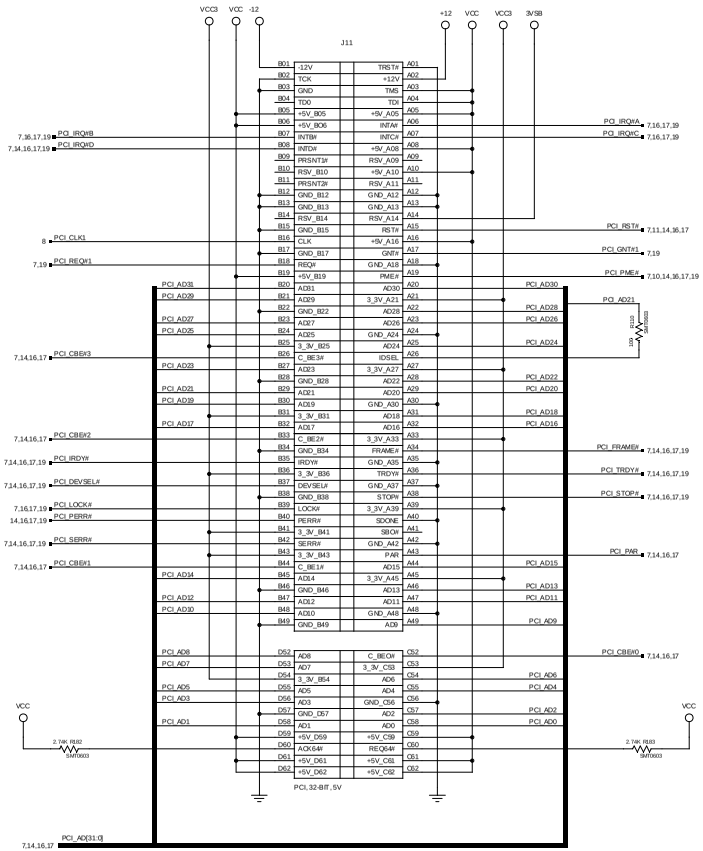
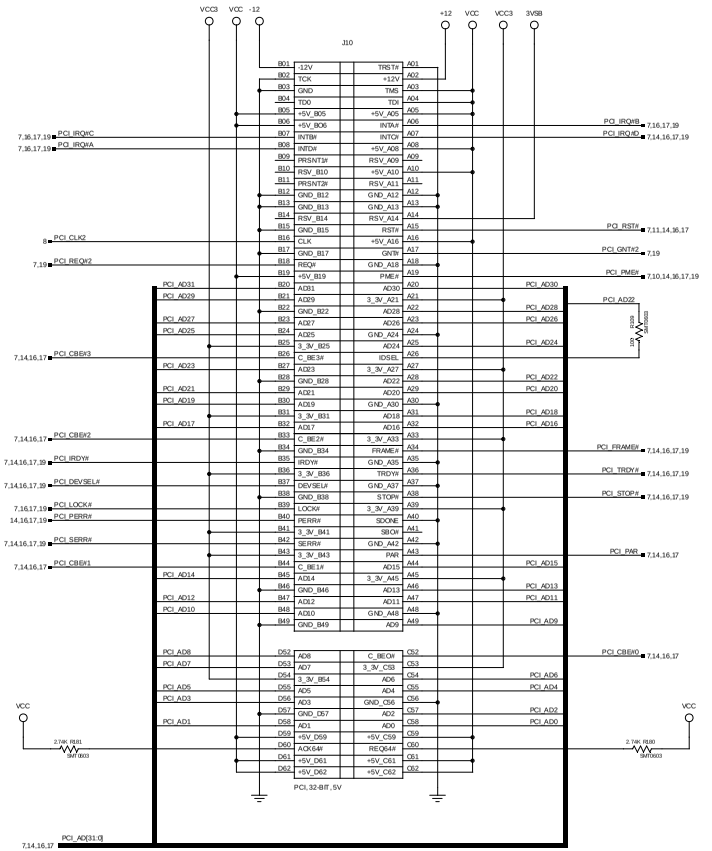
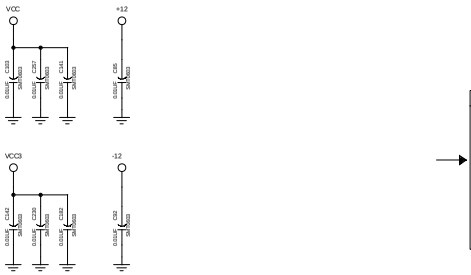
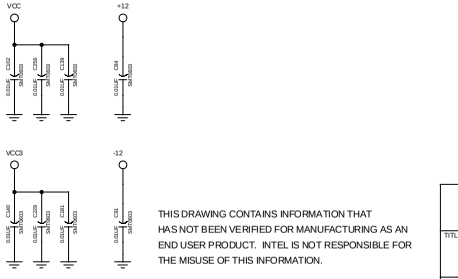






PCI RESOURCES

SLOT	DEV NUM	IDSEL	INT[A,B,C,D]#	PCICLK	REQ[0:N]#
440MX	7	AD18	A, B, C, D	0	n/a
ENET	4	AD15	D, A, B, C	4	0
SLOT 1	10	AD21	A, B, C, D	1	1
SLOT 2	11	AD22	B, C, D, A	2	2
SLOT 3	12	AD23	C, D, A, B	3	3



PCI RESOURCES

SLOT	DEV NUM	IDSEL	INT[A,B,C,D]#	PCICLK	REQ[0:N]#
440MX	7	AD18	A, B, C, D	0	n/a
ENET	4	AD15	D, A, B, C	4	0
SLOT 1	10	AD21	A, B, C, D	1	1
SLOT 2	11	AD22	B, C, D, A	2	2
SLOT 3	12	AD23	C, D, A, B	3	3

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TITLE: PCI CONNECTORS 1 AND 2

REV: B

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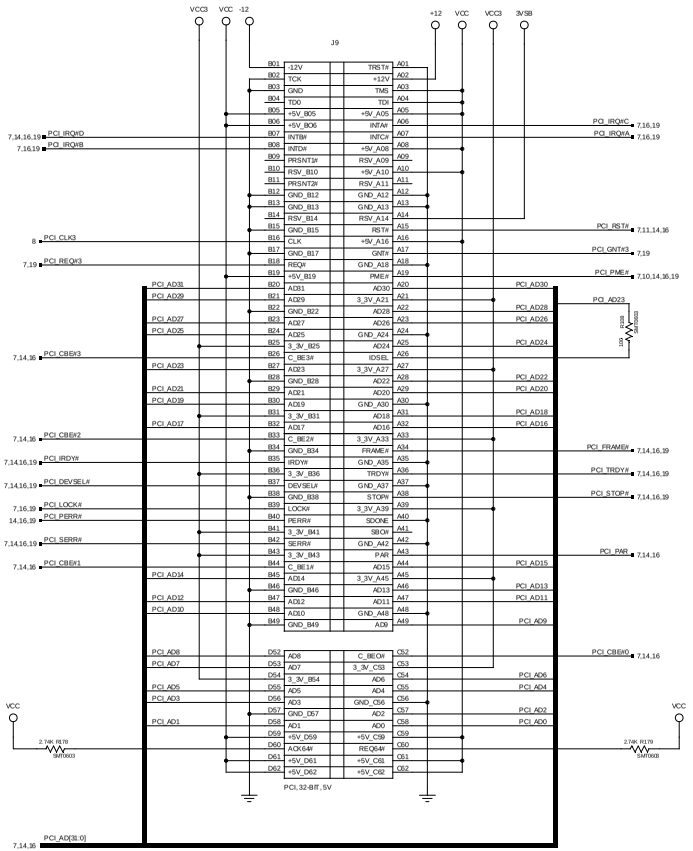
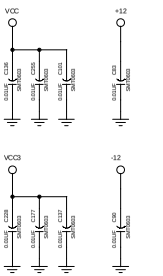
DRAWING: 440MX SCALABLE LOW POWER BOARD

SHEET: 16 OF 19





PCI RESOURCES

SLOT	DEV NUM	IDSEL	INT[A,B,C,D]#	P/CCLK	REQ/GNT
440MX	7	AD18	A, B, C, D	0	n/a
ENET	4	AD15	D, A, B, C	4	0
SLOT 1	10	AD21	A, B, C, D	1	1
SLOT 2	11	AD22	B, C, D, A	2	2
SLOT 3	12	AD23	C, D, A, B	3	3

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TITLE: PCI CONNECTOR 3

REV: B

LAST: 09/20/01 10:29 AM

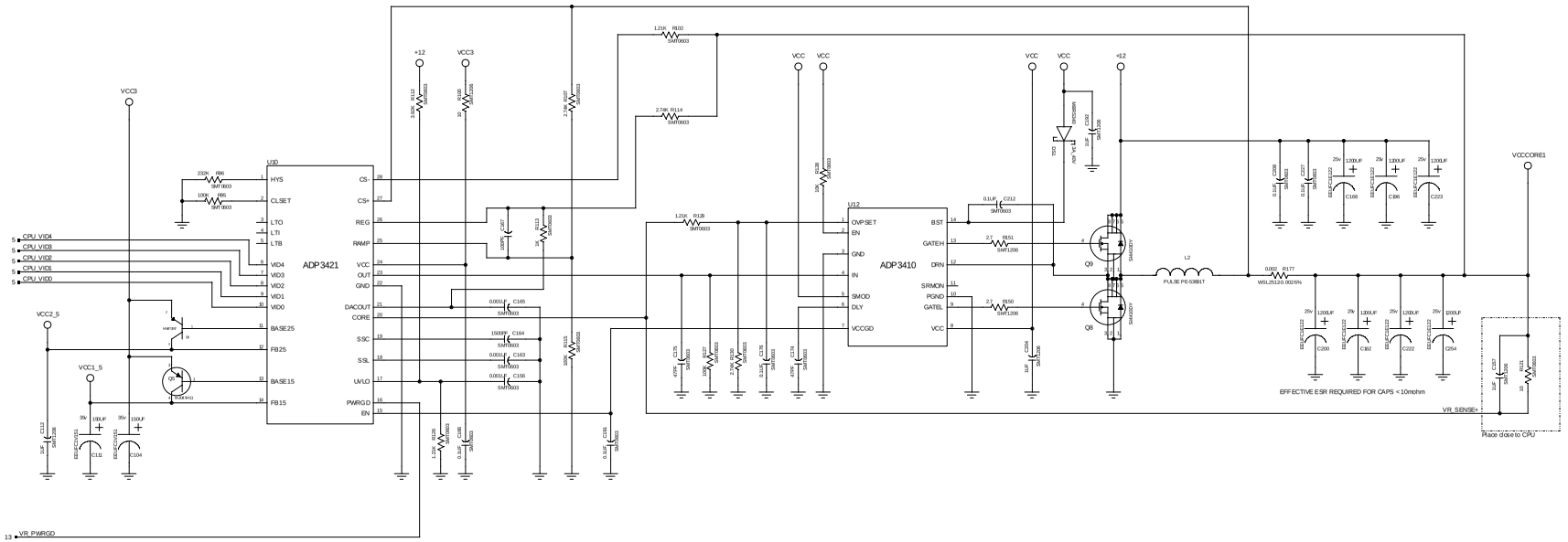
DATE: 09/18/01

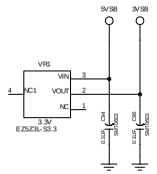
DRAWING: B 440MX SCALABLE LOW POWER BOARD

SHEET: 17 OF 19

ROUTING NOTES - POWER SUPPLY

1. Distance from MOSFETs to driver IC should be as small as placement allows
2. Connection between components in the high current path must be sized to handle 25A
3. Add multiple vias where high current traces switch layers to reduce resistance and inductance and improve heat dissipation
4. Avoid routing any signals, including power supply control signals, over the switching power path loop
5. The core voltage sense resistor and parallel capacitor must be located close to the CPU, but far from the switcher





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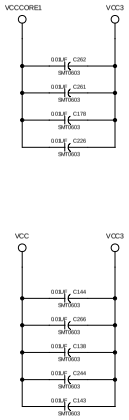
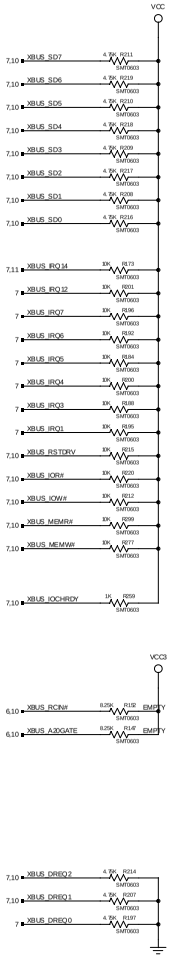
TITLE: VOLTAGE REGULATORS		REV: B	
		LAST: 09/20/01 10:29 AM	
DATE: 09/18/01	B	DRAWING: 440MX SCALABLE LOW POWER BOARD	SHEET: 18 OF 19

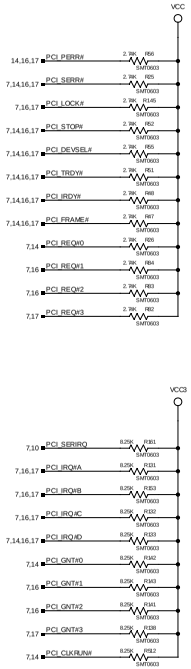
POWER PLANE DECOUPLING



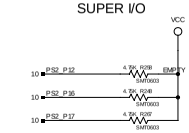
XBUS



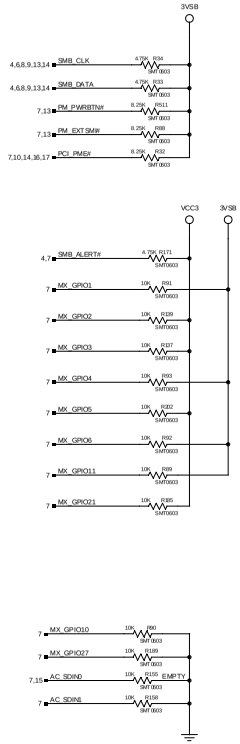
PCI BUS



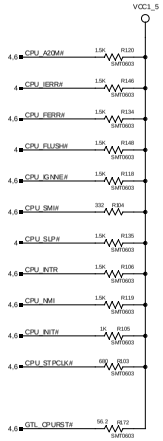
SUPER I/O

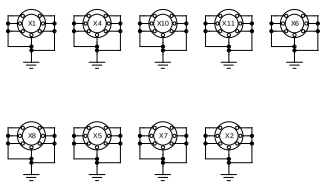


MX CHIPSET



GTL+ BUS





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TITLE: PULLUP/PULLDOWN RESISTORS		REV: B	
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